BURR-BROWN®

ADS931

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SpeedPLUS™ 8-Bit, 33MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- +2.7V TO +5.5V SUPPLY OPERATION
- LOW POWER: 69mW at +3V
- ADJUSTABLE FULL SCALE RANGE WITH EXTERNAL REFERENCE
- NO MISSING CODES
- POWER DOWN
- SSOP-28 PACKAGE

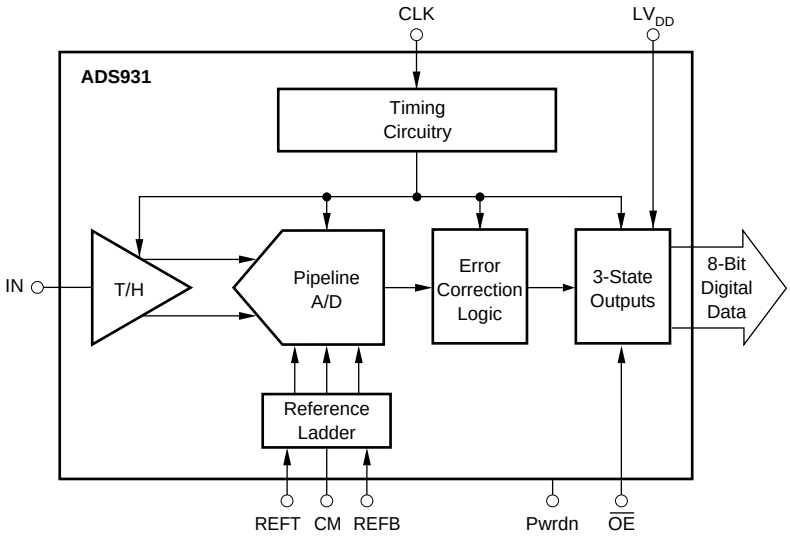
APPLICATIONS

- BATTERY POWERED EQUIPMENT
- CAMCORDERS
- PORTABLE TEST EQUIPMENT
- DIGITAL CAMERAS
- COMMUNICATIONS

DESCRIPTION

The ADS931 is a high speed pipelined analog-to-digital converter that is specified to operate from standard +5V or +3V power supplies. This converter includes a high bandwidth track/hold and an 8-bit quantizer. The performance is specified with a single-ended input range of 1V to 2V when operating off of a +3V supply. This device also allows for standard input ranges such as 2V to 4V or 2V to 3V, when operating on +5V supplies. The full scale input range is set by an external reference.

The ADS931 employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for telecommunications, video and test instrumentation applications. The ADS931 is available in a SSOP-28 package.



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SPECIFICATIONS

At T_A = full specified temperature range unless otherwise noted. $+V_S = LV_{DD}$ = +3V, specified single-ended input (1V to 2V) and sampling rate = 30MHz, unless otherwise specified. The input range is 2.25V to 3.25V when specified for +5V operation.

PARAMETER	CONDITIONS	ADS931E MIN	ADS931E TYP	ADS931E MAX	UNITS
RESOLUTION			8		Bits
SPECIFIED TEMPERATURE RANGE	Ambient Air		–40 to +85		°C
ANALOG INPUT					
Specified Full Scale Input Range[1]	1Vp-p	+1.0		+2.0	V
Common-mode Voltage			+1.5		V
Analog Input Bias Current			1		µA
Input Impedance			1.25 || 5		MΩ || pF
DIGITAL INPUTS					
Logic Family			TTL/HCT Compatible CMOS		
High Input Voltage, V_{IH}		+2.0		LV_{DD}	V
Low Input Voltage, V_{IL}				+0.8	V
High Input Current, I_{IH}			±10		µA
Low Input Current, I_{IL}			±10		µA
Input Capacitance			5		pF
CONVERSION CHARACTERISTICS					
Start Conversion			Rising Edge of Convert Clock		
Sample Rate		10k		33M	Samples/s
Data Latency			5		Clk Cycles
DYNAMIC CHARACTERISTICS					
Differential Linearity Error	V_S = +3V and +5V				
f = 500kHz			±0.7	±1.0	LSB
f = 12.5MHz			±0.7		LSB
No Missing Codes	V_S = +3V and +5V		Guaranteed		
Integral Nonlinearity Error, f = 500kHz	V_S = +3V and +5V		±1.0	±2.5	LSB
Spurious Free Dynamic Range[2]	V_S = +3V and +5V				
f = 500kHz (–1dBFS input)			49		dBFS[3]
f = 12.5MHz (–1dBFS input)		43	49		dBFS
Two-Tone Intermodulation Distortion[4]					
f = 3.6MHz and 3.5MHz (–7dBFS each tone)			54		dBFS
Signal-to-Noise Ratio (SNR)	V_S = +3V and +5V				
f = 500kHz (–1dBFS input)			48		dB
f = 12.5MHz (–1dBFS input)		44	48		dB
Signal-to-(Noise + Distortion) (SINAD)	V_S = +3V and +5V				
f = 500kHz (–1dBFS input)			45		dB
f = 12.5MHz (–1dBFS input)		40	45		dB
Effective Number of Bits	f = 12MHz[5]		7.2		Bits
Differential Gain Error	NTSC, PAL		2.3		%
Differential Phase Error	NTSC, PAL		1		degrees
Output Noise	Input AC-Grounded		0.2		LSBs rms
Aperture Delay Time			2		ns
Aperture Jitter			7		ps rms
Analog Input Bandwidth					
Small Signal	–20dBFS Input		350		MHz
Full Power	0dBFS Input		100		MHz
Overvoltage Recovery Time[6]			2		ns
DIGITAL OUTPUTS	C_L = 15pF				
Logic Family			TTL/HCT Compatible CMOS		
Logic Coding			Straight Offset Binary		
High Output Voltage, V_{OH}		2.4		V_{DD}	V
Low Output Voltage, V_{OL}				0.4	V
3-State Enable Time	$\overline{OE}$ = L		20	40	ns
3-State Disable Time	$\overline{OE}$ = H		2	10	ns
Internal Pull-Down			50		kΩ
Power-Down Enable Time	Pwrdn = L		133		ns
Power-Down Disable Time	Pwrdn = H		18		ns
Internal Pull-Down			50		kΩ
ACCURACY	V_S = +3V and +5V				
Gain Error			2.4	3.5	%FS
Input Offset[7]	Referred to Ideal Midscale		±6.5	±25	mV
Power Supply Rejection (Gain)	ΔV_S = +10%		75		dB
External REFT Voltage Range		REFB +0.5	2	V_S–0.8	V
External REFB Voltage Range		0.8	1	REFT –0.5	V
Reference Input Resistance				4	kΩ

SPECIFICATIONS (Cont.)

At T_A = full specified temperature range unless otherwise noted. $+V_S = LV_{DD} = +3V$, specified single-ended input (1V to 2V) and sampling rate = 30MHz, unless otherwise specified. The input range is 2.25V to 3.25V when specified for +5V operation.

PARAMETER	CONDITIONS	ADS931E			UNITS
		MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS					
Supply Voltage: $+V_S$	Operating	+2.7	+3.0	+5.5	V
Supply Current: $+I_S$	V_S = +3V		23	29	mA
Power Dissipation	V_S = +3V		69	87	mW
	V_S = +5V		154		mW
Power Dissipation (Power Down)	V_S = +3V		10		mW
	V_S = +5V		15		mW
Thermal Resistance, θ_{JA}					
28-Lead SSOP			89		°C/W

NOTES: (1) The single-ended input range is set by REFB and REFT values. (2) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (3) dBFS is dB relative to full scale. (4) Two-tone intermodulation distortion is referred to as the largest fundamental tone. (5) Based on (SINAD –1.76)/6.02. (6) No "Rollover" of bits. (7) Offset deviation from ideal negative full scale.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ ..... +6V
Analog Input ..... (–0.3V) to ($+V_S$ +0.3V)
Logic Input ..... (–0.3V) to ($+V_S$ +0.3V)
Case Temperature ..... +100°C
Junction Temperature ..... +150°C
Storage Temperature ..... +150°C

DEMO BOARD ORDERING INFORMATION

PRODUCT	DEMO BOARD
ADS931E	DEM-ADS9xxE

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS931E	SSOP-28 Surface Mount	324	–40°C to +85°C	ADS931E	ADS931E	Rails
"	"	"	"	"	ADS931E/1K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS931E/1K" will get a single 1000-piece Tape and Reel.

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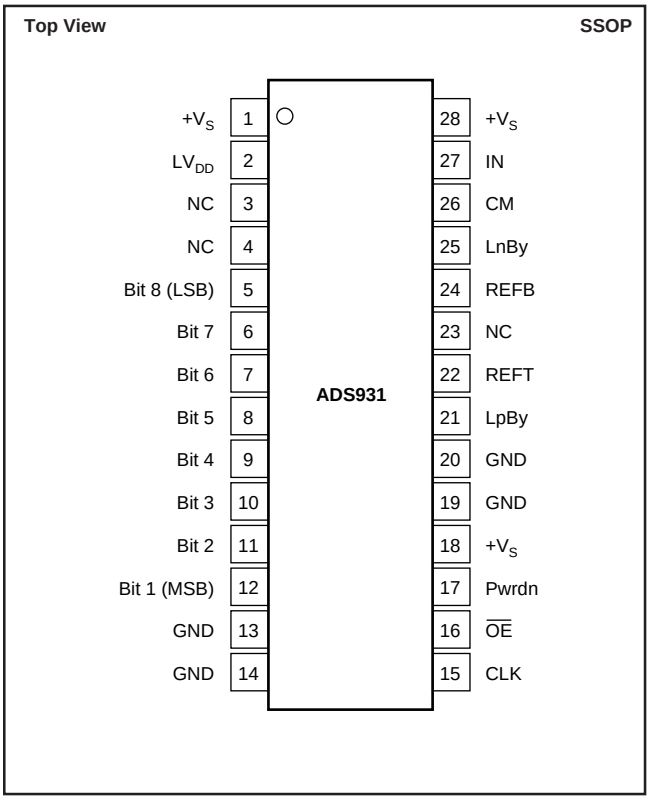
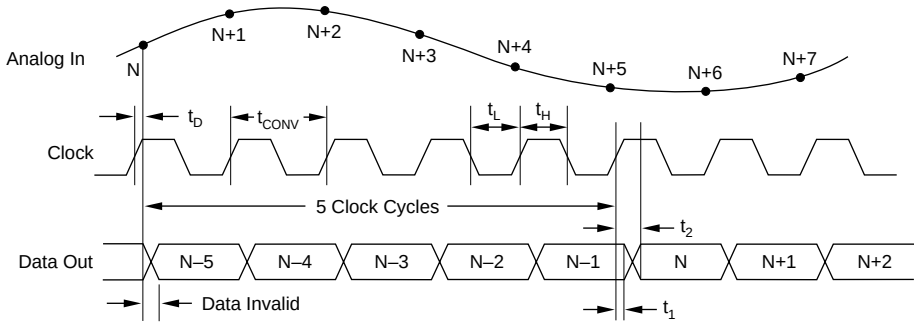
PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	DESIGNATOR	DESCRIPTION
1	$+V_S$	Analog Supply
2	LV_{DD}	Output Logic Driver Supply Voltage
3	NC	No Connection
4	NC	No Connection
5	Bit 8 (LSB)	Data Bit 8 (D7) LSB
6	Bit 7	Data Bit 7 (D6)
7	Bit 6	Data Bit 6 (D5)
8	Bit 5	Data Bit 5 (D4)
9	Bit 4	Data Bit 4 (D3)
10	Bit 3	Data Bit 3 (D2)
11	Bit 2	Data Bit 2 (D1)
12	Bit 1 (MSB)	Data Bit 1 (D0) MSB
13	GND	Analog Ground
14	GND	Analog Ground
15	CLK	Convert Clock Input
16	$\overline{OE}$	Output Enable, Active Low
17	Pwrdn	Power Down Pin
18	$+V_S$	Analog Supply
19	GND	Analog Ground
20	GND	Analog Ground
21	LpBy	Positive Ladder Bypass
22	REFT	Reference Voltage Top
23	NC	No Connection
24	REFB	Reference Voltage Bottom
25	LnBy	Negative Ladder Bypass
26	CM	Common-Mode Pin
27	IN	Analog Input
28	$+V_S$	Analog Supply

TIMING DIAGRAM

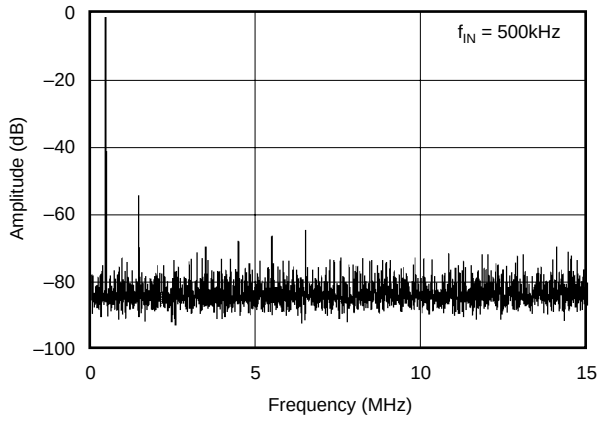


SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Convert Clock Period	30		100µs	ns
t_L	Clock Pulse Low	14	15		ns
t_H	Clock Pulse High	14	15		ns
t_D	Aperture Delay		2		ns
t_1	Data Hold Time, C_L = 0pF	3.9			ns
t_2	New Data Delay Time, C_L = 15pF max			12	ns

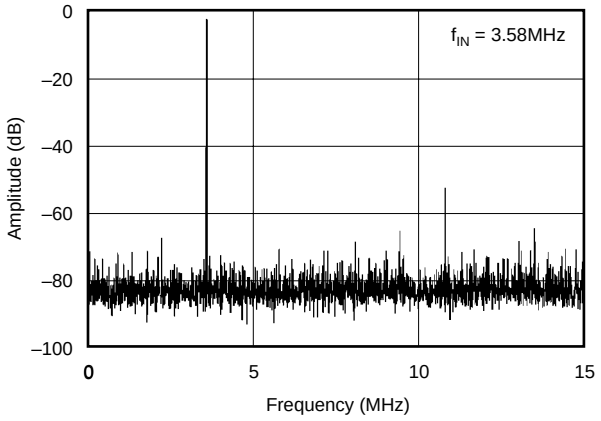
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +3V, specified single-ended input (–1dBFS) and sampling rate = 30MHz, unless otherwise specified.

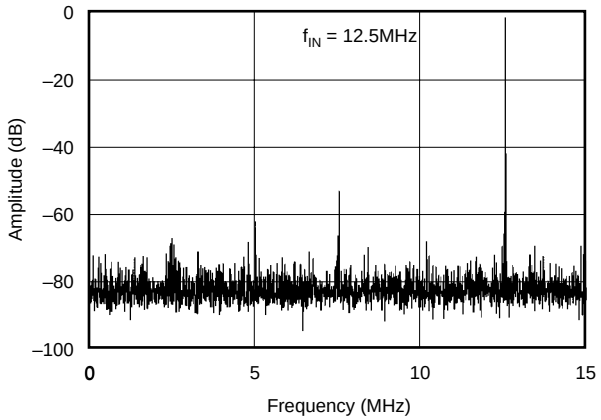
SPECTRAL PERFORMANCE



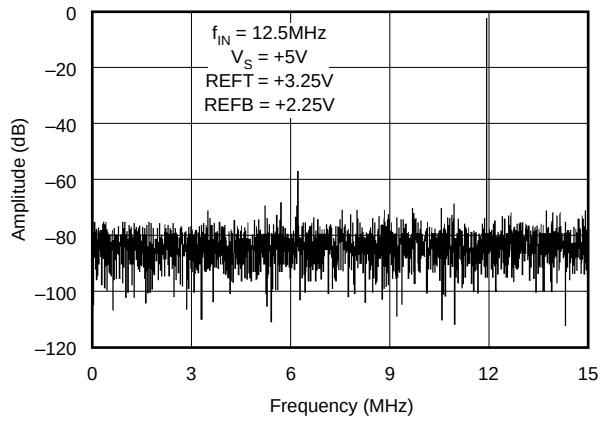
SPECTRAL PERFORMANCE



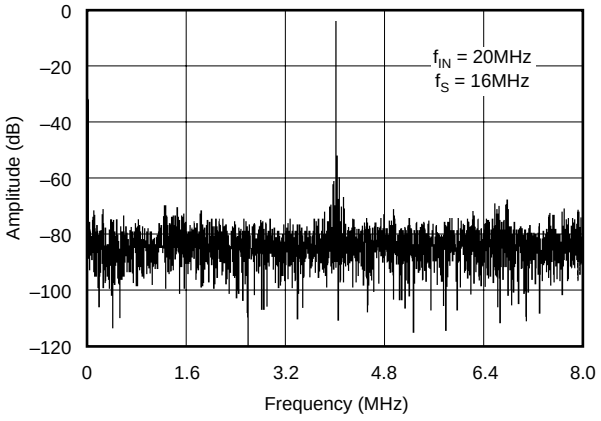
SPECTRAL PERFORMANCE



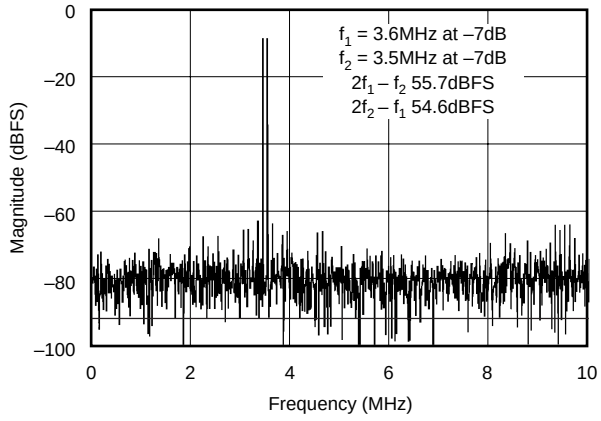
SPECTRAL PERFORMANCE



UNDERSAMPLING PERFORMANCE



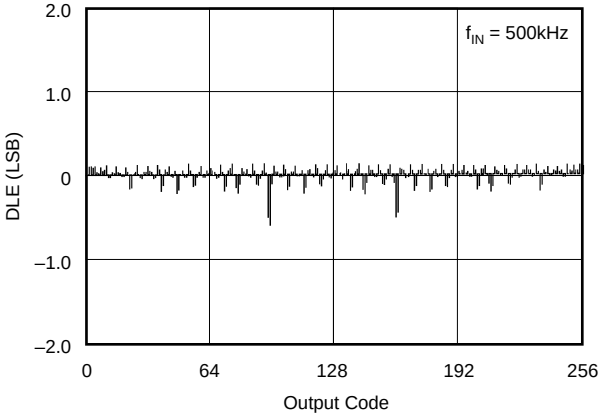
TWO-TONE INTERMODULATION



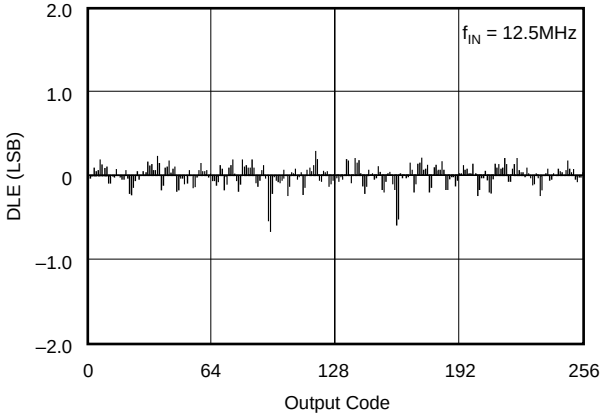
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = +3V, specified single-ended input (–1dBFS) and sampling rate = 30MHz, unless otherwise specified.

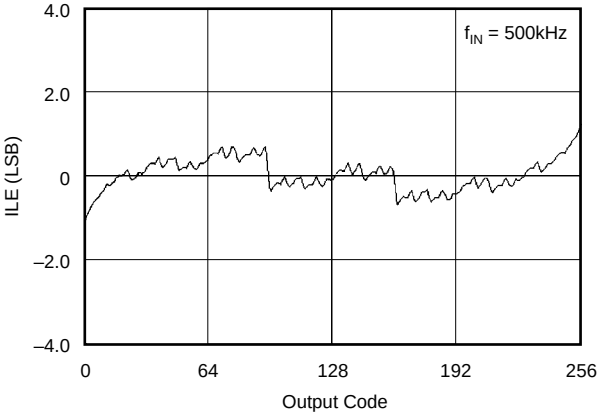
DIFFERENTIAL LINEARITY ERROR



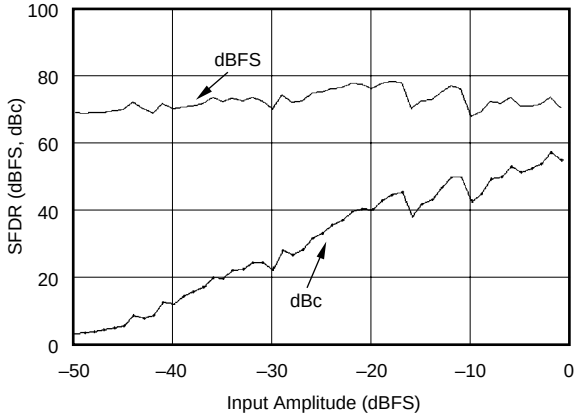
DIFFERENTIAL LINEARITY ERROR



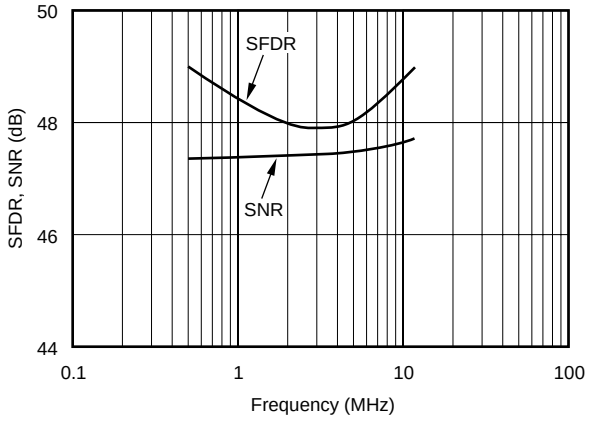
INTEGRAL LINEARITY ERROR



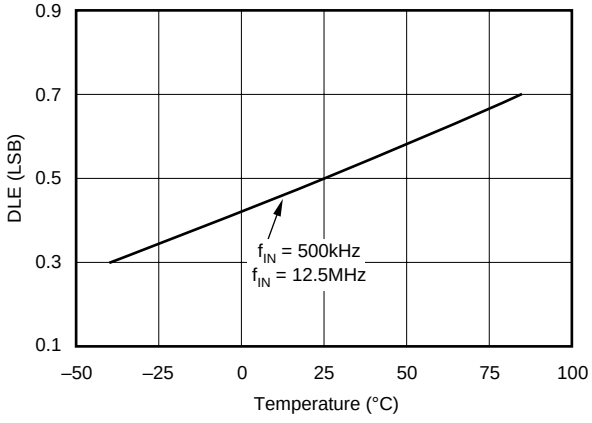
SWEPT POWER SFDR



DYNAMIC PERFORMANCE vs INPUT FREQUENCY



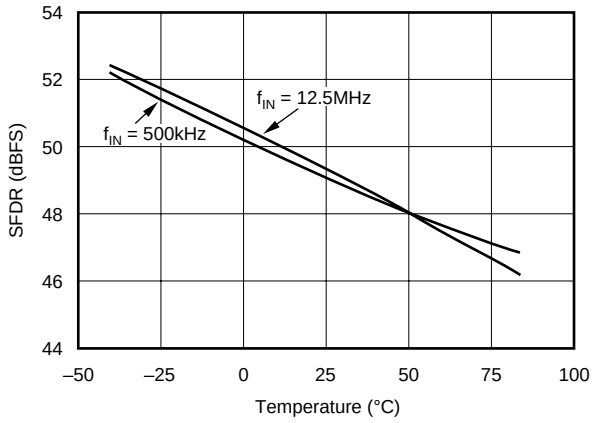
DIFFERENTIAL LINEARITY ERROR
vs TEMPERATURE



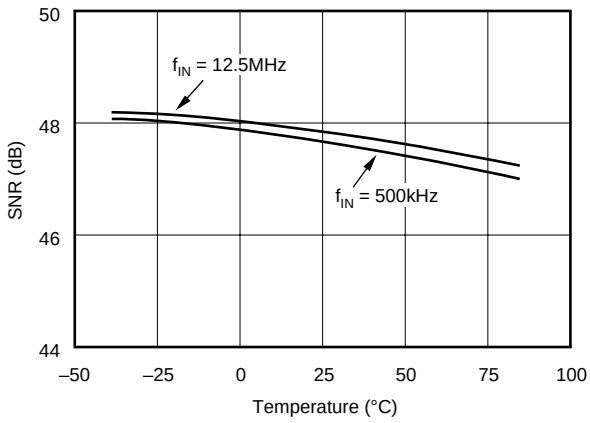
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = +3V, specified single-ended input (–1dBFS) and sampling rate = 30MHz, unless otherwise specified.

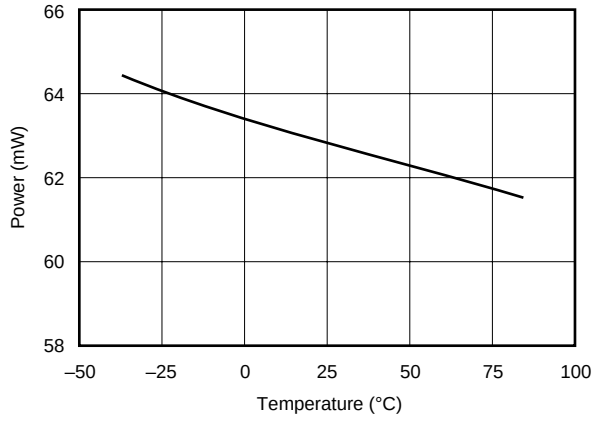
SPURIOUS FREE DYNAMIC RANGE (SFDR) vs TEMPERATURE



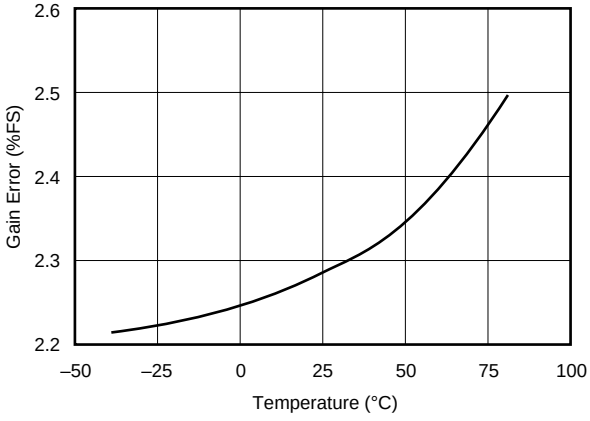
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



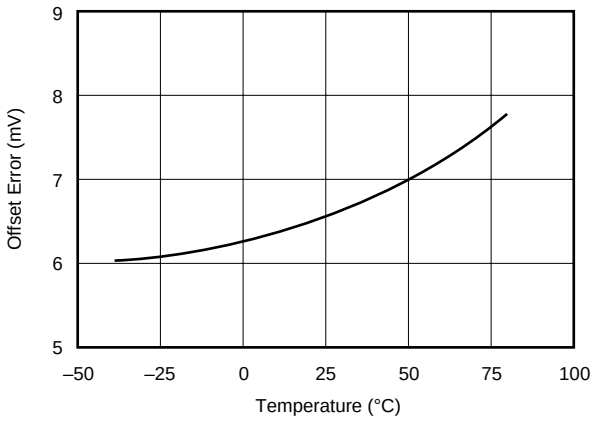
POWER DISSIPATION vs TEMPERATURE



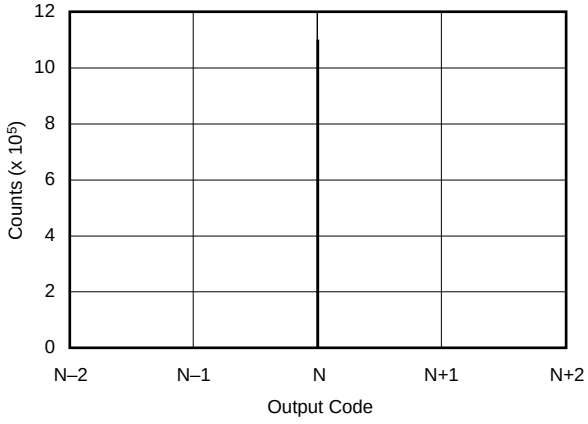
GAIN ERROR vs TEMPERATURE



OFFSET ERROR vs TEMPERATURE



OUTPUT NOISE HISTOGRAM (DC Input)



THEORY OF OPERATION

The ADS931 is a high speed sampling analog-to-digital converter that utilizes a pipeline architecture. The fully differential topology and digital error correction guarantee 8-bit resolution. The track/hold circuit is shown in Figure 1. The switches are controlled by an internal clock which has a non-overlapping two phase signal, ϕ1 and ϕ2. At the sampling time the input signal is sampled on the bottom plates of the input capacitors. In the next clock phase, ϕ2, the bottom plates of the input capacitors are connected together and the feedback capacitors are switched to the op amp output. At this time the charge redistributes between C_I and C_H, completing one track/hold cycle. The differential output is a held DC representation of the analog input at the sample time. In the normal mode of operation, the complementary input is tied to the common-mode voltage. In this case, the track/hold circuit converts a single-ended input signal into a fully differential signal for the quantizer. Consequently, the input signal gets amplified by a gain or two, which improves the signal-to-noise performance. Other parameters such as small-signal and full-power bandwidth, and wideband noise are also defined in this stage.

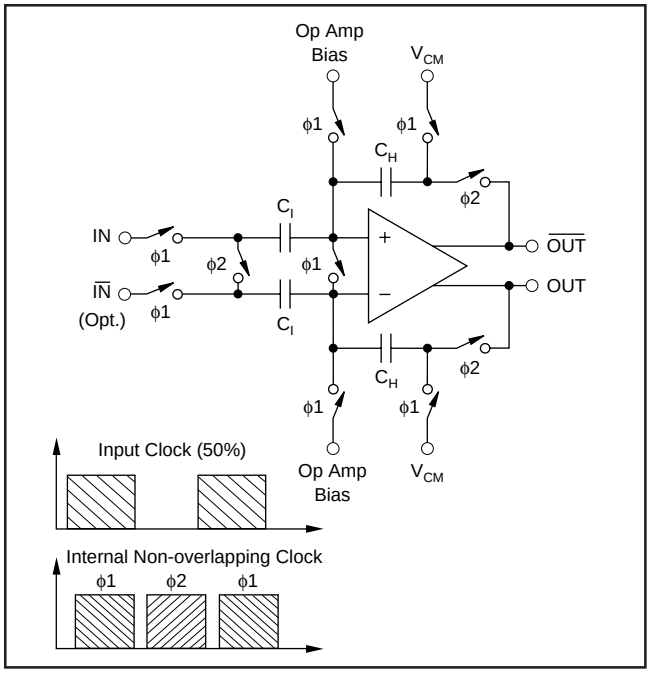


FIGURE 1. Input Track/Hold Configuration with Timing Signals.

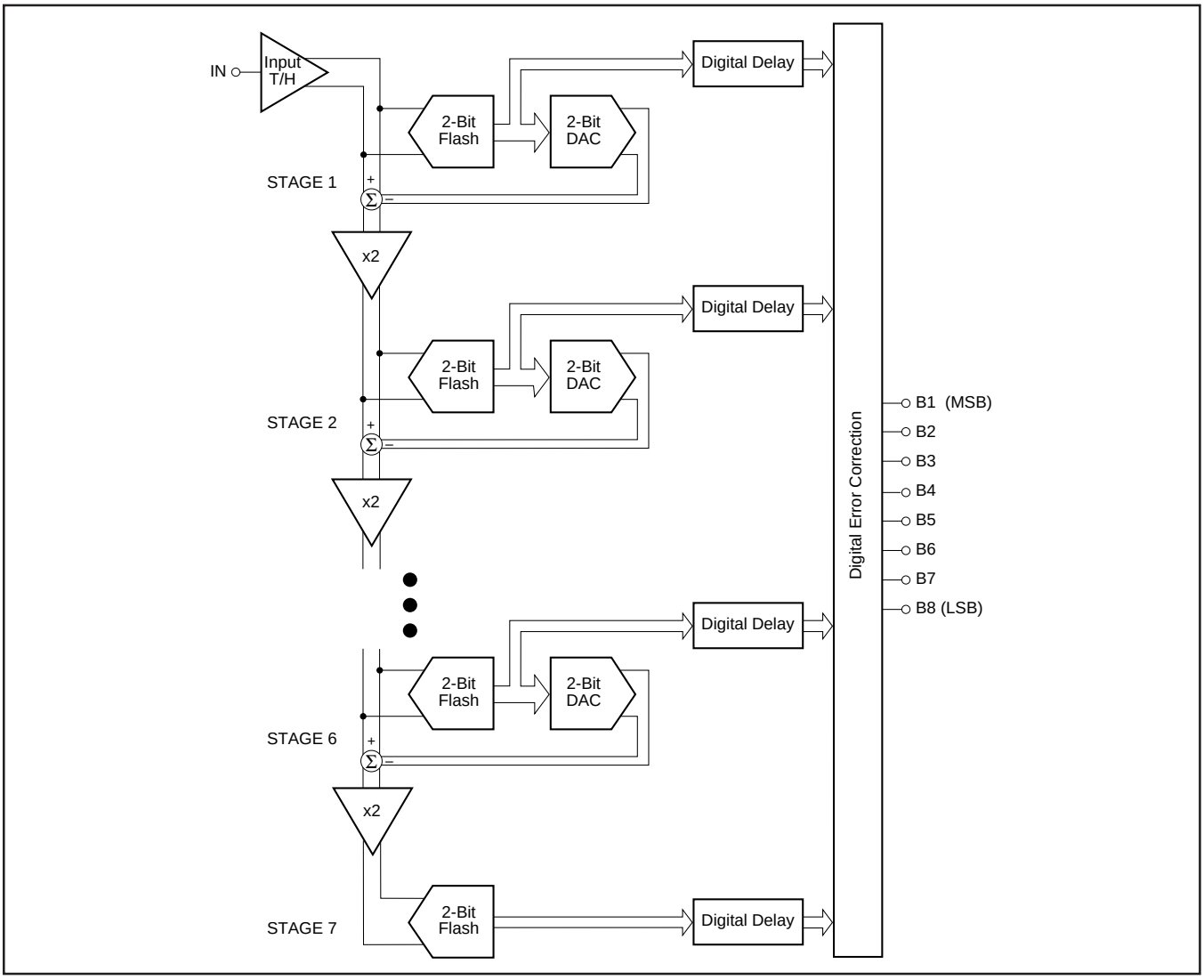


FIGURE 2. Pipeline A/D Architecture.

The pipelined quantizer architecture has 7 stages with each stage containing a two-bit quantizer and a two bit digital-to-analog converter, as shown in Figure 2. Each two-bit quantizer stage converts on the edge of the sub-clock, which is the same frequency of the externally applied clock. The output of each quantizer is fed into its own delay line to time-align it with the data created from the subsequent quantizer stages. This aligned data is fed into a digital error correction circuit which can adjust the output data based on the information found on the redundant bits. This technique provides the ADS931 with excellent differential linearity and guarantees no missing codes at the 8-bit level.

To accommodate a bipolar signal swing, the ADS931 operates with a common-mode voltage (V_{CM}) which is derived from the external references. Due to the symmetric resistor ladder inside the ADS931, V_{CM} is situated between the top and bottom reference voltage. Equation (1) can be used for calculating the common-mode voltage level.

$$V_{CM} = (REFT + REFB)/2 \quad (1)$$

At the same time, the two external reference voltage levels define the full-scale input range for the ADS931. This makes it possible for the input range to be adapted to the signal swing of the front end.

APPLICATIONS

SIGNAL SWING AND COMMON-MODE CONSIDERATIONS

The ADS931 is primarily designed and specified for a +3V single supply voltage. However, due to its supply range of +2.7V to +5.25V, it is well suited for +5V applications. The nominal input signal swing is 1Vp-p, situated between +1V and +2V. This means that the signal swings ±0.5V around a common-mode voltage of +1.5V when using a 3V rail, or typically +2.75V on a 5V supply. In some applications, it might be advantageous to increase the input signal swing. For example, increasing it to 2Vp-p may improve the achievable signal-to-noise performance. However, consideration should be given to keeping the signal swing within the linear range of operation of the driving circuitry to avoid any excessive distortion. In extreme situations, the performance of the converter will start to degrade due to large variations of the input's switch ON resistance over the input voltage. Therefore, the signal swing should remain approximately 0.5V away from each rail during normal operation.

DRIVING THE ANALOG INPUTS AC-COUPLED DRIVER

Figure 3 shows an example of an ac-coupled, single-ended interface circuit using a high speed op amp which operates on dual supplies (OPA650, OPA658). The mid-point reference voltage, (V_{CM}), biases the bipolar, ground-referenced input signal. The capacitor C_1 and resistor R_1 form a high-pass filter with the –3dB frequency set at

$$f_{-3dB} = 1/(2\,\pi\,R_1\,C_1) \quad (2)$$

The values for C_1 and R_1 are not critical in most applications and can be set freely. The values shown in Figure 3 correspond to a corner frequency of 1.6kHz.

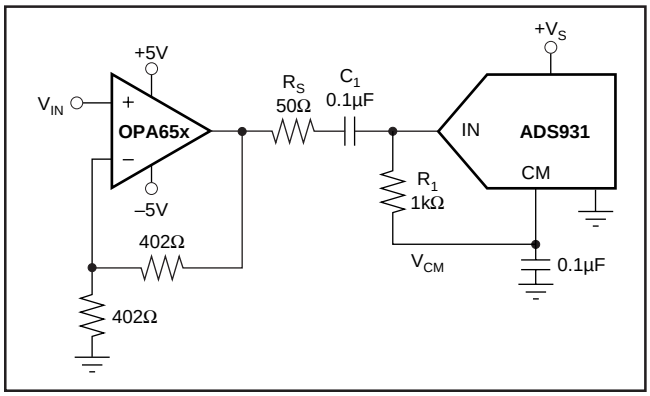


FIGURE 3. AC-Coupled, Single-Ended Interface Circuit.

Figure 4 depicts a circuit that can be used in single-supply applications. The mid-reference voltage biases the op amp up to the appropriate common-mode voltage, for example V_{CM} = +1.5V. With the use of capacitor C_G, the DC gain for the non-inverting op amp input is set to +1V/V. As a result, the transfer function is modified to

$$V_{OUT} = V_{IN}\,\{(1 + R_F/R_G) + V_{CM}\} \quad (3)$$

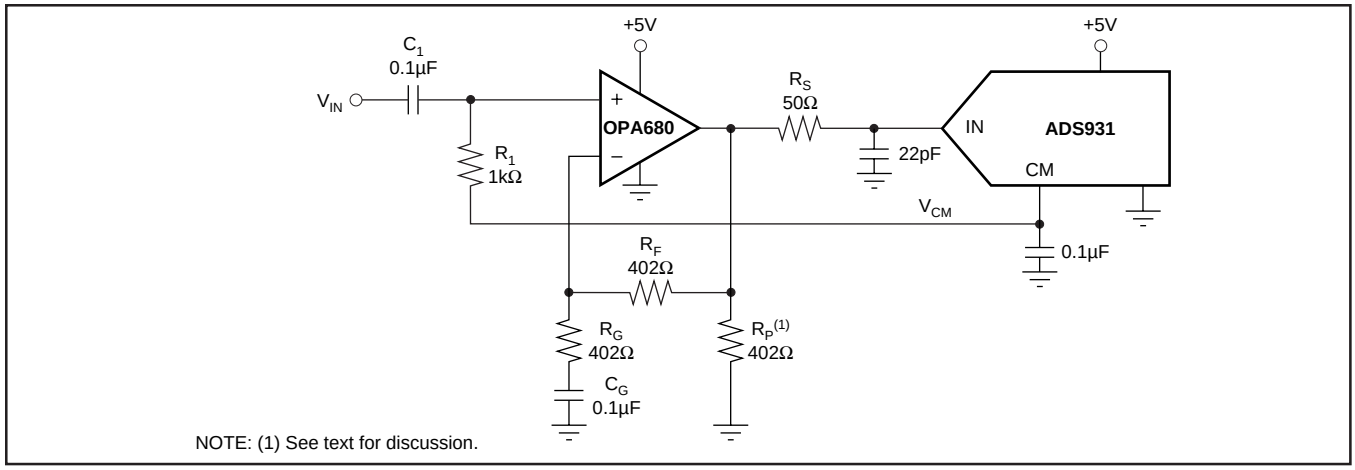


FIGURE 4. +5V Single-Supply Interface Circuit Example Using the Voltage Feedback Amplifier OPA680.

Again, the input coupling capacitor C_1 and resistor R_1 form a high-pass filter. At the same time, the input impedance is defined by R_1. Although many high-speed op amps operate on single supply voltages down to +3V, their ac-performance is often lower when compared to their +5V ac-performance. This is especially true at signal frequencies of 5MHz or higher, where noticeable degradation is exhibited that will limit the performance of the system. If possible, the op amp and A/D converter pair should be supplied with +5V and the common-mode voltage set to +2.5V, which is usually the preferred dc bias level for single-supply op amps. Keeping the signal swing within 1Vp-p prevents the op amp from exhibiting excessive distortion caused by its slew-rate limitations. Depending on the selected amplifier, the use of a pull-up or pull-down resistor (R_P) located directly at its output may considerably improve the distortion performance. Resistor R_S isolates the op amp's output from the capacitive load to avoid gain peaking or even oscillation. It can also be used to establish a defined bandwidth in order to roll off the high frequency noise. The value of R_S is usually set between 10Ω and 100Ω.

DC-COUPLED INTERFACE CIRCUIT

Shown in Figure 5 is a single-supply, DC-coupled circuit which can be set in a gain of –1V/V or higher. Depending on the gain, the divider ratio set by resistors R_1 and R_2 must be adjusted to yield the correct common-mode voltage for the ADS931. With a +3V supply, the input signal of the ADS931 is 1Vp-p, typically centered around the common-mode voltage of +1.5V, which can be derived from the external references.

EXTERNAL REFERENCE

The ADS931 requires external references on pin 22 (REFT) and pin 24 (REFB). Internally those pins are connected by the resistor ladder, which has a nominal resistance of 4kΩ (±15%). In order to establish a correct voltage drop across the ladder, the external reference circuit must be able to supply typically 250µA of current. With this current the full-scale input range of the ADS931 is set between +1V and +2V, or 1Vp-p. In general, the voltage drop across REFT and REFB determines the input full-scale range (FSR) of the ADS931. Equation (4) can be used to calculate the span.

$$FSR = REFT - REFB \quad (4)$$

Depending on the application, several options are possible to supply the external reference voltages to the ADS931 without degrading the typical performance.

LOW-COST SOLUTION

The easiest way to achieve the required reference voltages is to place the reference ladder of the ADS931 between the supply rails, as shown in Figure 6. Two additional resistors (R_T, R_B) are necessary to set the correct current through the ladder. The table in Figure 6 lists the value for several possible configurations, however depending on the desired full-scale swing and supply voltage, different resistor values might be selected.

The trade-offs, when selecting this reference circuit, are the variations in the reference voltages due to component tolerances, temperature drift and power supply variations. In any case, it is recommended to bypass the reference ladder with at least 0.1µF ceramic capacitors, as shown in Figure 6. The purpose of the capacitors is twofold. They will bypass most of the high frequency noise which results from feedthrough of the clock and switching noise from the sample and hold stages. Secondly, they serve as a charge reservoir to supply instantaneous current to internal nodes.

HIGH ACCURACY SOLUTION

For those application demanding a higher level of dc accuracy and drift a reference circuit with a precision reference element might be used (see Figure 7). A stable +1.2V

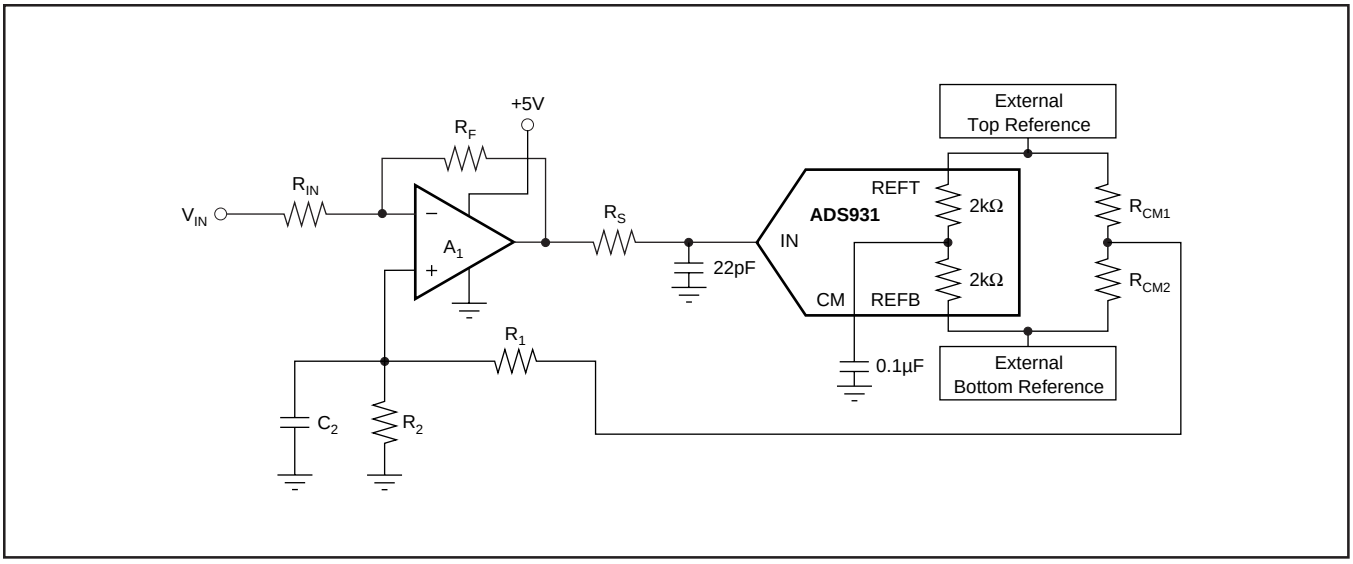
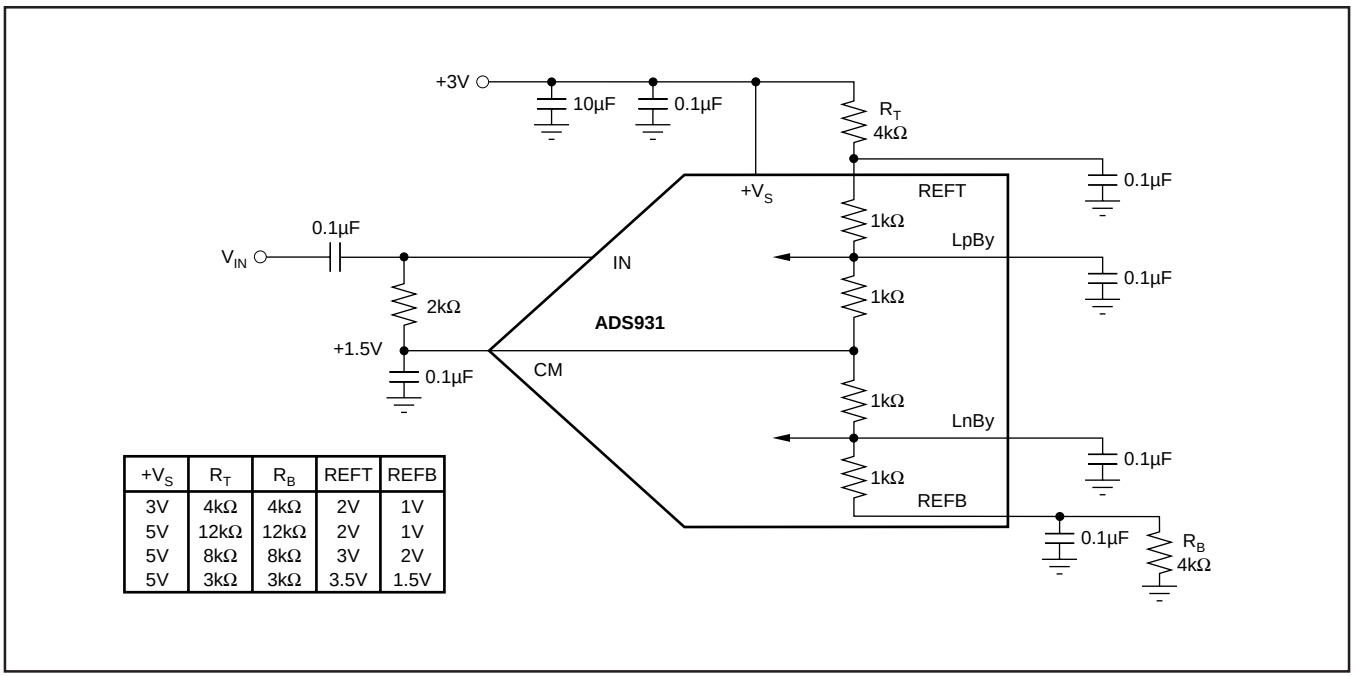


FIGURE 5. Single-Ended, DC-Coupled Interface Circuit.



$+V_S$	R_T	R_B	REFT	REFB
3V	4kΩ	4kΩ	2V	1V
5V	12kΩ	12kΩ	2V	1V
5V	8kΩ	8kΩ	3V	2V
5V	3kΩ	3kΩ	3.5V	1.5V

FIGURE 6. Low-cost Solution to Supply External Reference Voltages.

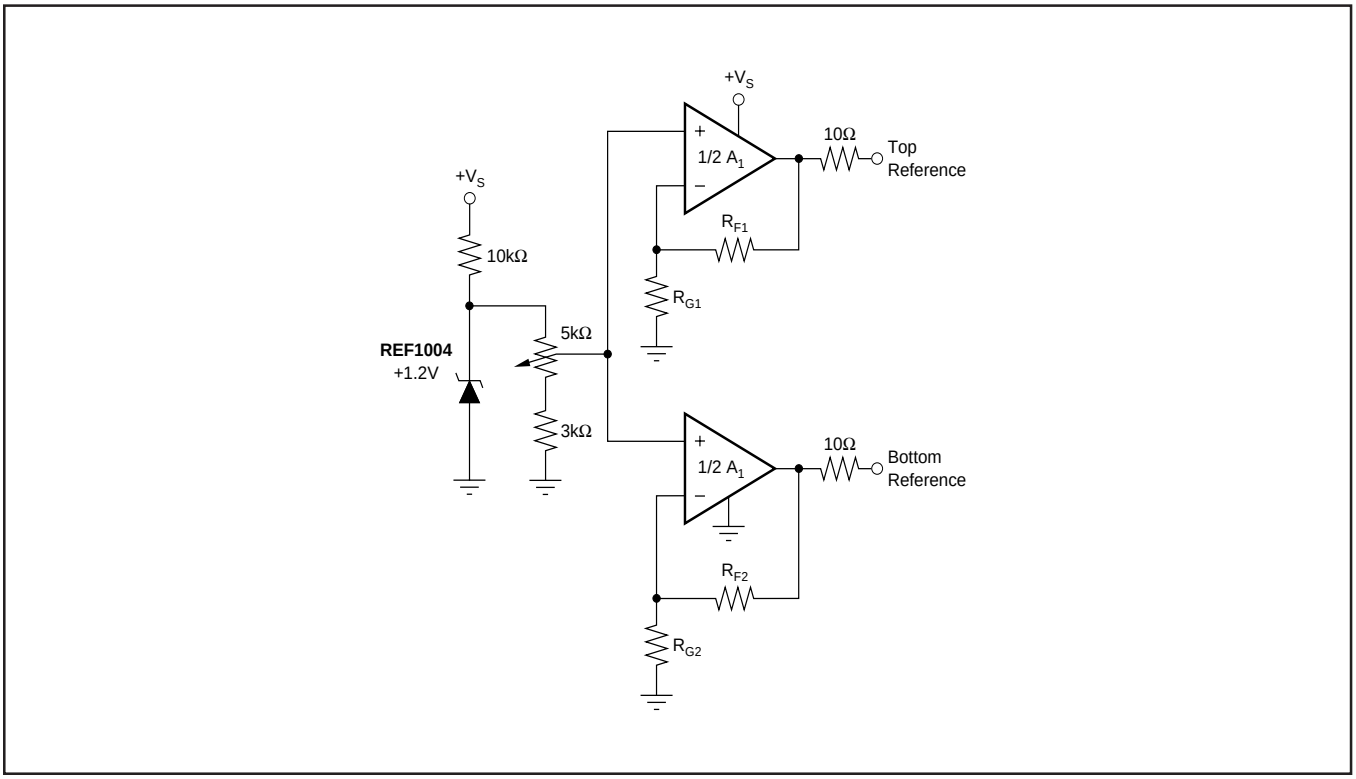


FIGURE 7. High Accuracy Solution to Supply External Reference Voltages.

reference voltage is established by a two terminal bandgap reference diode, the REF1004-1.2. Using a general-purpose single-supply dual operational amplifier (A_1), like an OPA2237, OPA2234 or MC34072, the two required reference voltages for the ADS931 can be generated by setting each op amp to the appropriate gain; for example: set REFT to +2V and REFB to +1V.

CLOCK INPUT

The clock input of the ADS931 is designed to accommodate either +3V or +5V CMOS logic levels. To drive the clock input with a minimum amount of duty cycle variation and support the maximum sampling rate (30MSPS), high speed or advanced CMOS logic should be used (HC/HCT, AC/ACT). When digitizing at high sampling rates, a 50%

duty cycle, along with fast rise and fall times (2ns or less), are recommended to meet the rated performance specifications. However, the ADS931 performance is tolerant to duty cycle variations of as much as ±10%, which should not affect the performance. For applications operating with input frequencies up to Nyquist ($f_{CLK}/2$) or undersampling applications, special consideration must be made to provide a clock with very low jitter. Clock jitter leads to aperture jitter (t_A) which can be the ultimate limitation to achieving good SNR performance. Equation (5) shows the relationship between aperture jitter, input frequency and the signal-to-noise ratio:

$$SNR = 20\log10\ [1/(2\ \pi\ f_{IN}\ t_A)] \quad (5)$$

DIGITAL OUTPUTS

The digital outputs of the ADS931 are standard CMOS stages and designed to be compatible to both high speed TTL and CMOS logic families. The logic thresholds are for low-voltage CMOS: V_{OL} = 0.4V, V_{OH} = 2.4V, which allows the ADS931 to directly interface to 3V logic. The digital output driver of the ADS931 uses a dedicated digital supply pin (pin 2, LV_{DD}), see Figure 8. By adjusting the voltage on LV_{DD}, the digital output levels will vary respectively. It is recommended to limit the fan-out to one in order to keep the capacitive loading on the data lines below the specified 15pF. If necessary, external buffers or latches may be used to provide the added benefit of isolating the A/D converter from any digital activities on the bus coupling back high frequency noise, which degrades the performance.

SINGLE-ENDED INPUT	STRAIGHT OFFSET BINARY (SOB) PIN 12 FLOATING or LO
+FS (IN = REFT Voltage)	11111111
+FS –1LSB	11111111
+FS –2LSB	11111110
+3/4 Full Scale	11100000
+1/2 Full Scale	11000000
+1/4 Full Scale	10100000
+1LSB	10000001
Bipolar Zero (IN +1.5V)	10000000
–1LSB	01111111
–1/4 Full Scale	01100000
–1/2 Full Scale	01000000
–3/4 Full Scale	00100000
–FS +1LSB	00000001
–FS (IN = REFB Voltage)	00000000

TABLE I. Coding Table for the ADS931.

POWER-DOWN MODE

The ADS931's low power consumption can be reduced even further by initiating a power-down mode. For this, the Power Down pin (pin 17) must be tied to a logic "High" reducing the current drawn from the supply by approximately 84%. In normal operation, the power-down mode is disabled by an internal pull-down resistor (50kΩ).

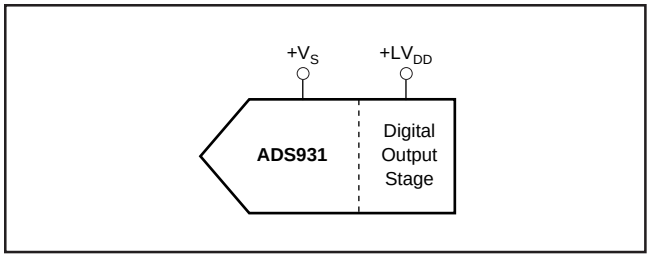


FIGURE 8. Independent Supply Connection for Output Stage.

During power-down, the digital outputs are set in 3-state. With the clock applied, the converter does not accurately process the sampled signal. After removing the power-down condition, the output data from the following 5 clock cycles is invalid (data latency).

DECOUPLING AND GROUNDING CONSIDERATIONS

The ADS931 has several supply pins, one of which is dedicated to supply only the output driver (LV_{DD}). The remaining supply pins are not divided into analog and digital supply pins ($+V_S$) since they are internally connected on the chip. For this reason, it is recommended that the converter be treated as an analog component and to power it only from the analog supply. Digital supply lines often carry high levels of noise which can couple back into the converter and limit performance.

Because of the pipeline architecture, the converter also generates high frequency transients and noise that are fed back into the supply and reference lines. This requires that the supply and reference pins be sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the analog supplies. In most cases, 0.1µF ceramic chip capacitors are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close as possible to the supply pins. In addition, one larger bipolar capacitor (1µF to 22µF) should be placed on the PC board in proximity of the converter circuit.

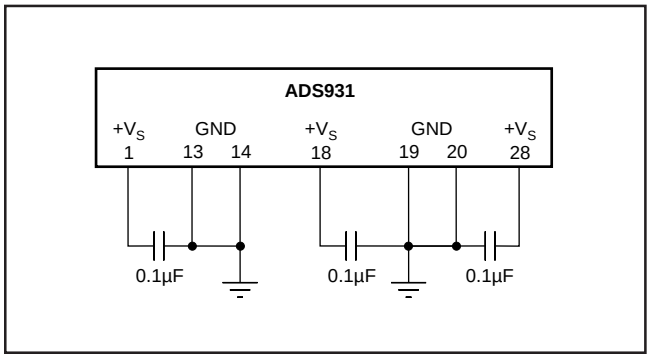


FIGURE 9. Recommended Bypassing for Analog Supply Pins.