



# 500kHz, 12-Bit, 6-Channel Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 6 SIMULTANEOUS SAMPLING CHANNELS
- FULLY DIFFERENTIAL INPUTS
- 2μs TOTAL THROUGHPUT PER CHANNEL
- GUARANTEED NO MISSING CODES
- PARALLEL INTERFACE
- 1MHz EFFECTIVE SAMPLING RATE
- LOW POWER: 50mW
- 6X FIFO

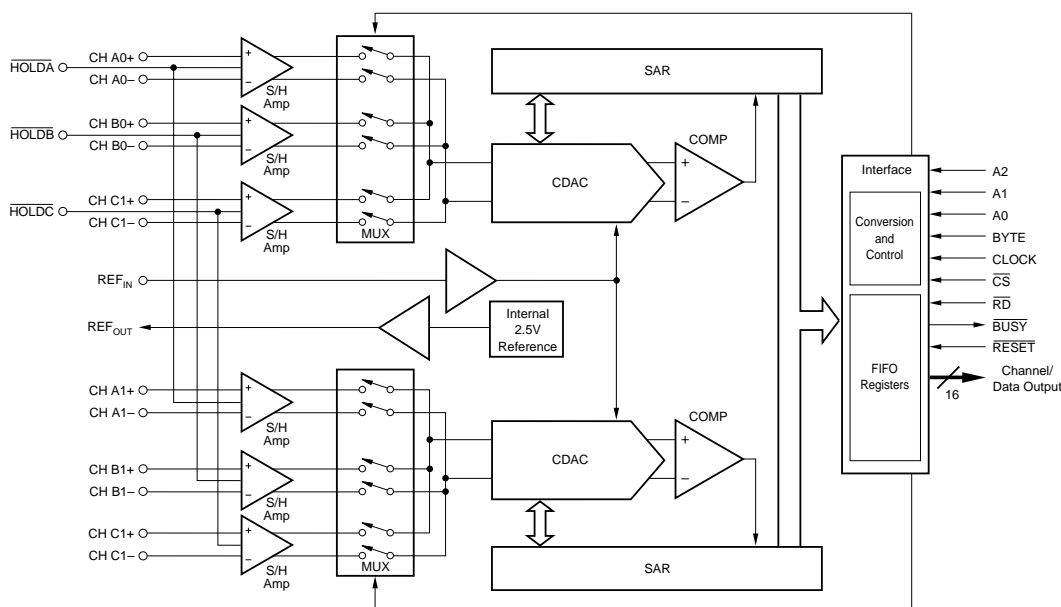
## APPLICATIONS

- MOTOR CONTROL
- MULTI-AXIS POSITIONING SYSTEMS
- 3-PHASE POWER CONTROL

## DESCRIPTION

The ADS7804 is a dual 12-bit, 500kHz Analog-to-Digital (A/D) converter with 6 fully differential input channels grouped into three pairs for high speed simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the A/D converter. This provides excellent common-mode rejection of 80dB at 50kHz which is important in high noise environments.

The ADS7864 offers a parallel interface and control inputs to minimize software overhead. The output data for each channel is available as a 16-bit word (address and data). The ADS7864 is offered in a TQFP-48 package and is fully specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  operating range.



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# SPECIFICATIONS

All specifications  $T_{MIN}$  to  $T_{MAX}$ ,  $+V_A = +V_D = +5V$ ,  $V_{REF} = \text{internal } +2.5V$  and  $f_{CLK} = 8MHz$ ,  $f_{SAMPLE} = 500kHz$ , unless otherwise noted.

PARAMETER	CONDITIONS	ADS7864Y			ADS7864YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>				12			*	Bits
<b>ANALOG INPUT</b>								
Input Voltage Range-Bipolar	$V_{CENTER} = +2.5V$	$-V_{REF}$		$+V_{REF}$	*		*	V
Absolute Input Range	+IN	-0.3		$+V_A + 0.3$				V
	-IN	-0.3		$+V_A + 0.3$				V
Input Capacitance			15			*		pF
Input Leakage Current	CLK = GND		$\pm 1$			*		$\mu A$
<b>SYSTEM PERFORMANCE</b>								
No Missing Codes		12			*			Bits
Integral Linearity			$\pm 0.75$	$\pm 2$		$\pm 0.5$	$\pm 1$	LSB
Integral Linearity Match			0.5			*		LSB
Differential Linearity			$\pm 0.6$		*	$\pm 0.4$		LSB
Bipolar Offset Error	Referenced to $REF_{IN}$	-0.9	$\pm 0.75$	$\pm 4$		$\pm 0.5$	$\pm 3$	LSB
Bipolar Offset Error Match			3			*		LSB
Positive Gain Error	Referenced to $REF_{IN}$		$\pm 0.15$	$\pm 0.75$		$\pm 0.1$	$\pm 0.5$	% of FSR
Positive Gain Error Match			3			*		LSB
Negative Gain Error	Referenced to $REF_{IN}$		$\pm 0.15$	$\pm 0.75$		$\pm 0.1$	$\pm 0.5$	% of FSR
Negative Gain Error Match			3			*		LSB
Common-Mode Rejection Ratio	At DC		84			*		dB
	$V_{IN} = \pm 1.25V_{p-p}$ at 50kHz		80			*		dB
Noise			120			*		$\mu V_{rms}$
Power Supply Rejection Ratio			0.3	2		*	*	LSB
<b>SAMPLING DYNAMICS</b>								
Conversion Time per A/D			1.75			*		$\mu s$
Acquisition Time			0.25			*		$\mu s$
Throughput Rate		500			*			kHz
Aperture Delay			3.5			*		ns
Aperture Delay Matching			100			*		ps
Aperture Jitter			50			*		ps
Small-Signal Bandwidth			40			*		MHz
<b>DYNAMIC CHARACTERISTICS</b>								
Total Harmonic Distortion	$V_{IN} = \pm 2.5V_{p-p}$ at 100kHz		-75			*		dB
SINAD	$V_{IN} = \pm 2.5V_{p-p}$ at 100kHz		71			*		dB
Spurious Free Dynamic Range	$V_{IN} = \pm 2.5V_{p-p}$ at 100kHz		78			*		dB
Channel-to-Channel Isolation	$V_{IN} = \pm 2.5V_{p-p}$ at 50kHz		-76			*		dB
<b>VOLTAGE REFERENCE</b>								
Internal Reference Voltage		2.475	2.5	2.525	*	*	*	V
Internal Drift			10			*		ppm/ $^{\circ}C$
Internal Noise			50			*		$\mu V_{p-p}$
Internal Source Current			2			*		mA
Internal Load Rejection			0.005			*		mV/ $\mu A$
Internal PSRR			80			*		dB
External Reference Voltage Range		1.2	2.5	2.6	*	*	*	V
Input Current			100			*		$\mu A$
Input Capacitance			5			*		pF
<b>DIGITAL INPUT/OUTPUT</b>								
Logic Family			CMOS			*		
Logic Levels: $V_{IH}$	$I_{IH} = +5\mu A$	3.0		$+V_D + 0.3$	*		*	V
$V_{IL}$	$I_{IL} = +5\mu A$	-0.3		0.8	*		*	V
$V_{OH}$	$I_{OH} = -500\mu A$	3.5			*		*	V
$V_{OL}$	$I_{OL} = -500\mu A$			0.4			*	V
External Clock		0.2		8	*		*	MHz
Data Format		Binary Two's Complement				*		
<b>POWER SUPPLY REQUIREMENTS</b>								
Power Supply Voltage, $+V_A$ , $+V_D$		4.75	5	5.25	*	*	*	V
Quiescent Current, $+V_A$ , $+V_D$				10		*	*	mA
Power Dissipation				50		*	*	mW

\* Specifications same as ADS7864Y.

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## ABSOLUTE MAXIMUM RATINGS

Analog Inputs to AGND: Any Channel Input .....	-0.3V to (+V <sub>D</sub> + 0.3V)
REF <sub>IN</sub> .....	-0.3V to (+V <sub>D</sub> + 0.3V)
Digital Inputs to DGND .....	-0.3V to (+V <sub>D</sub> + 0.3V)
Ground Voltage Differences: AGND, DGND .....	±0.3V
+V <sub>D</sub> to AGND .....	-0.3V to +6V
Power Dissipation .....	325mW
Maximum Junction Temperature .....	+150°C
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

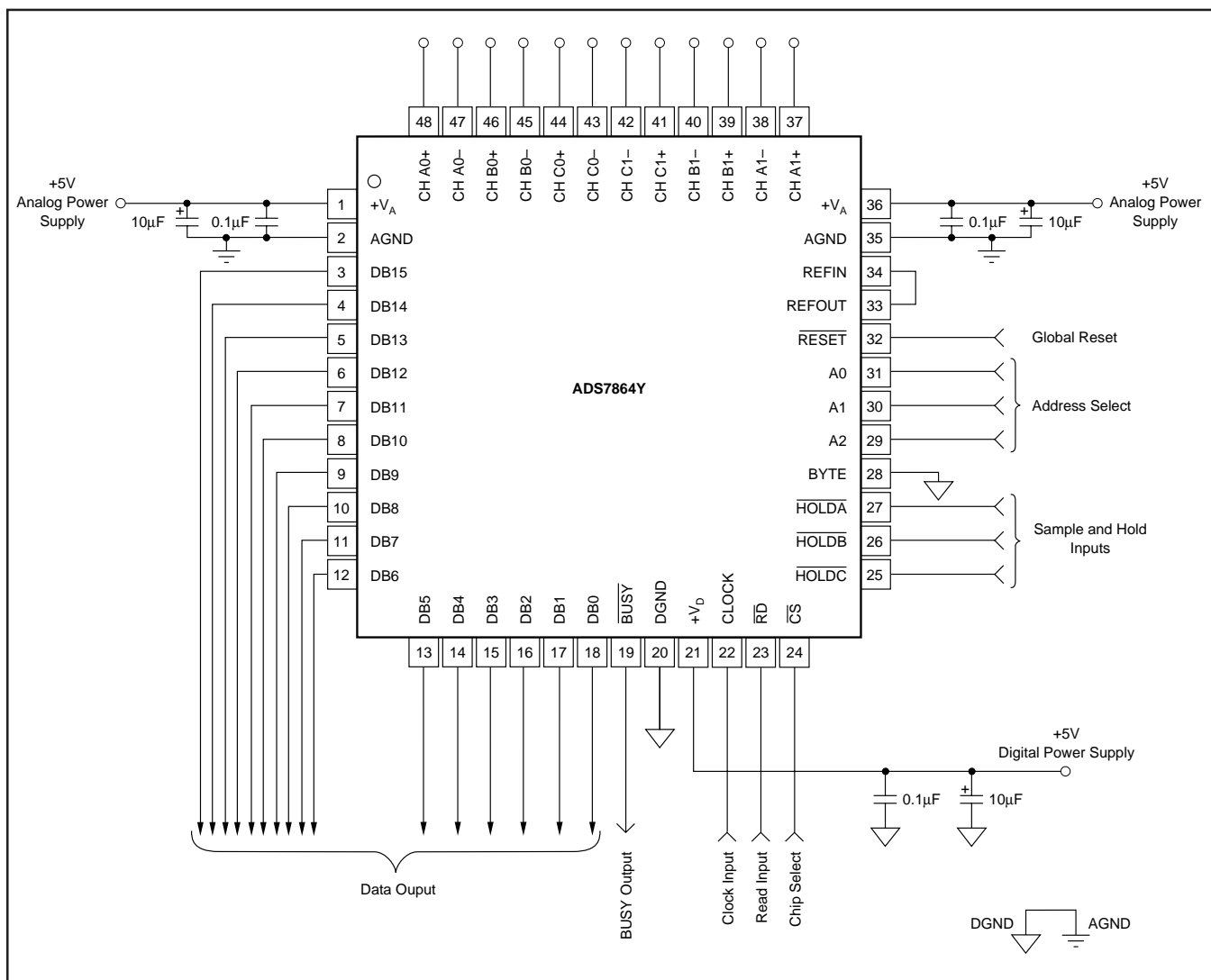
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

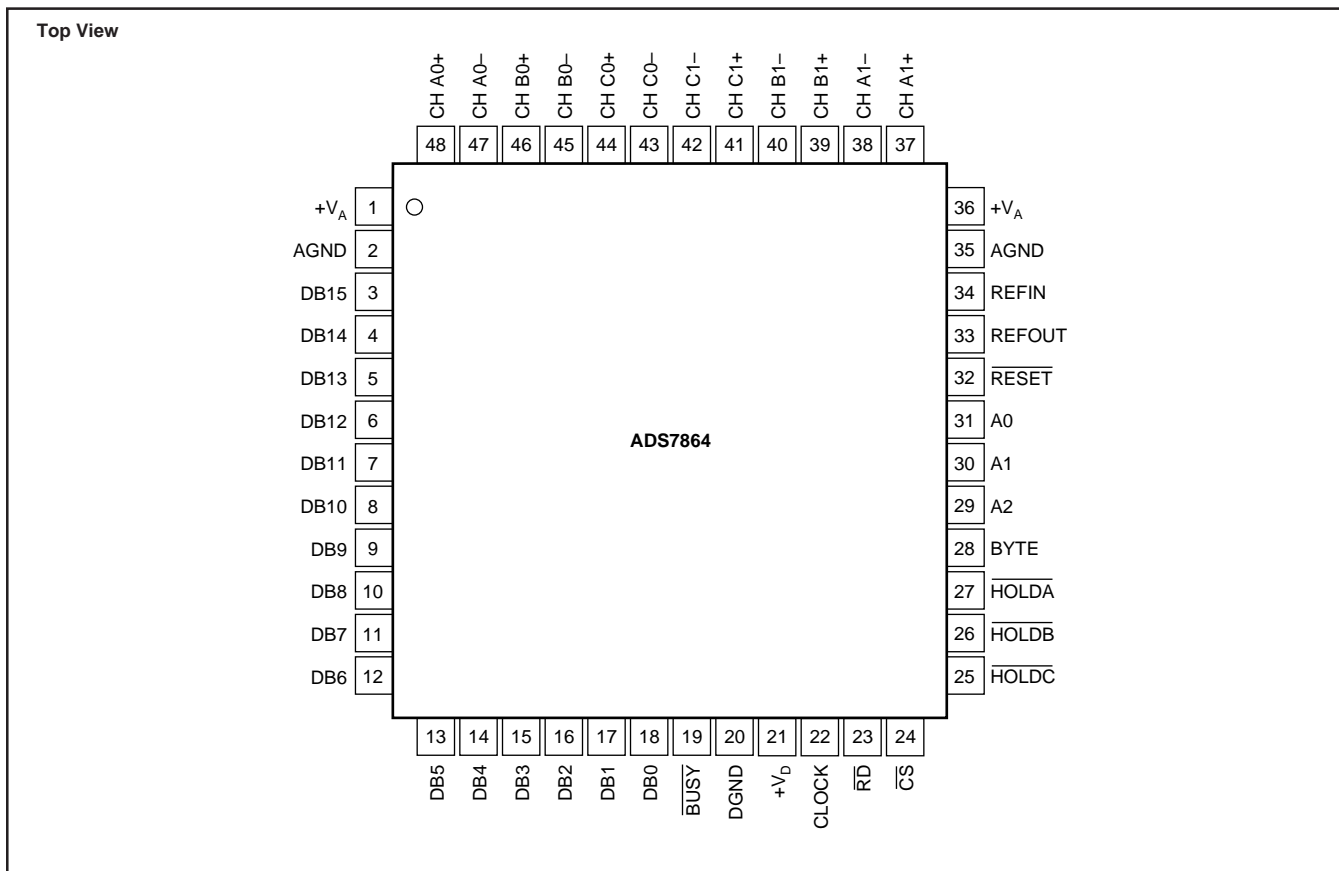
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (%)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER	ORDERING NUMBER (1)	TRANSPORT MEDIA
ADS7864Y	±2	±0.75	-40°C to +85°C	TQFP-48	355	ADS7864Y/250	Tape and Reel
"	"	"	"	"	"	ADS7864Y/2K	Tape and Reel
ADS7864YB	±1	±0.5	-40°C to +85°C	TQFP-48	355	ADS7864YB/250	Tape and Reel
"	"	"	"	"	"	ADS7864YB/2K	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "ADS7864Y/2K" will get a single 2000-piece Tape and Reel.

## BASIC OPERATION



## PIN CONFIGURATION

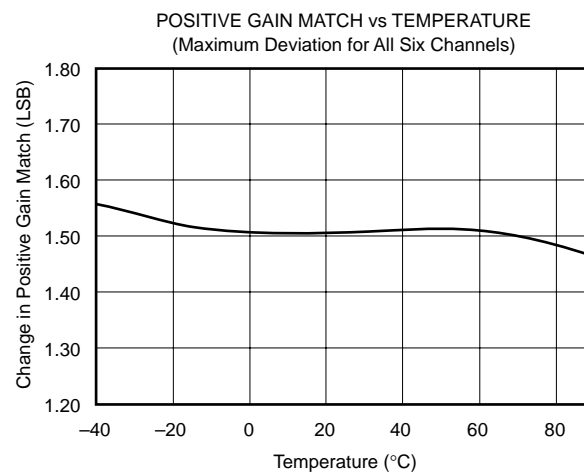
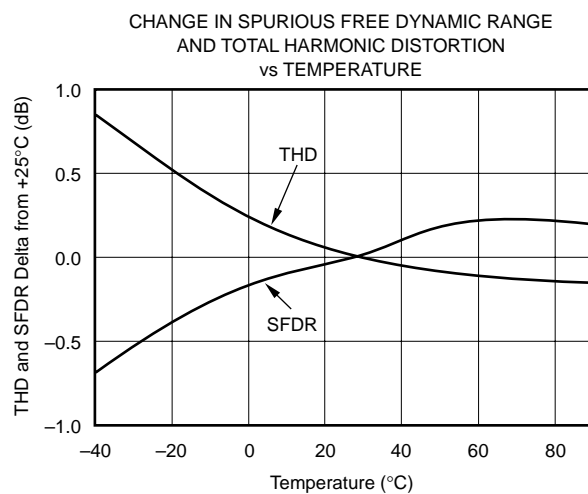
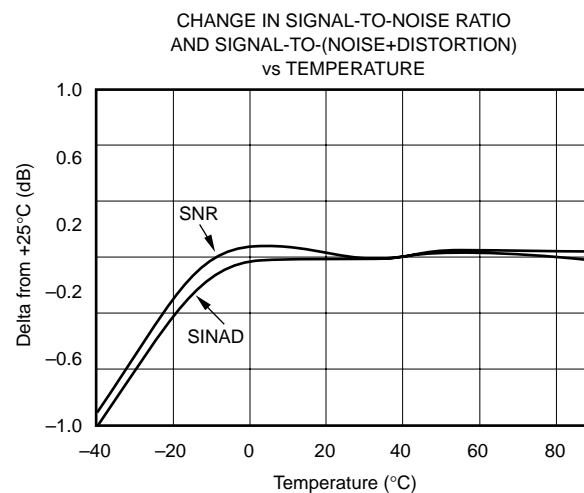
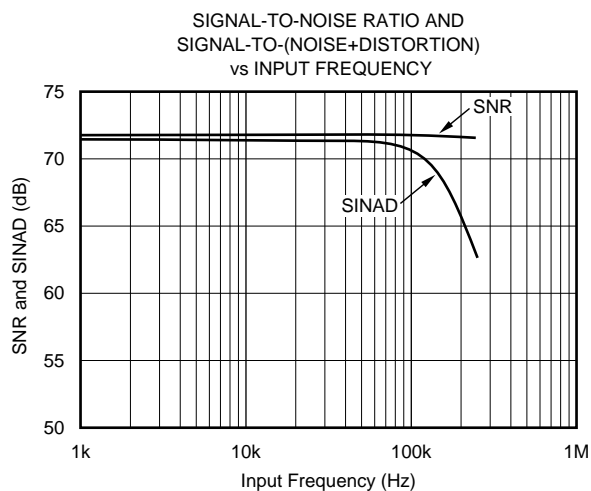
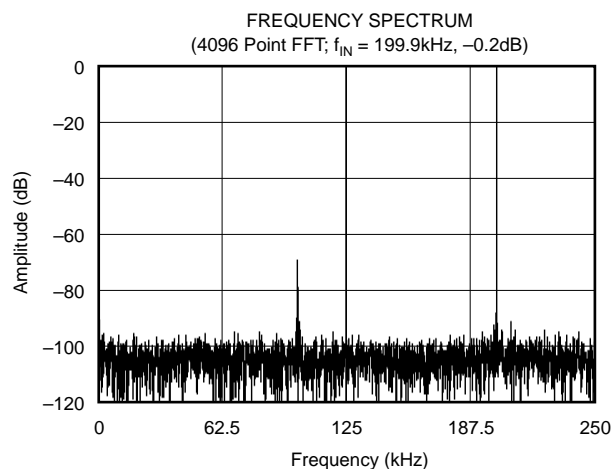
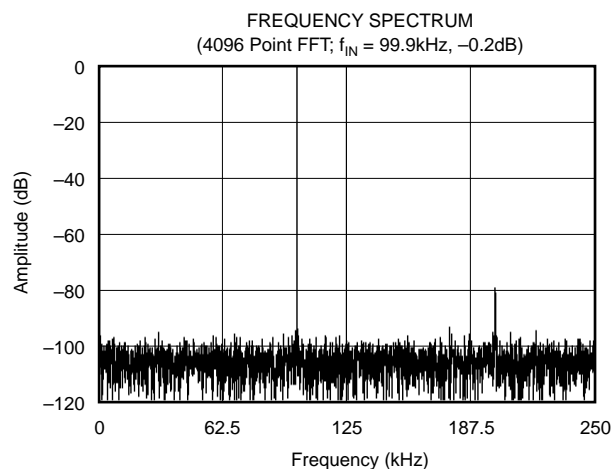


## PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	+V <sub>A</sub>	Analog Power Supply. Normally +5V.	25	HOLD $\overline{C}$	Places Channels C0 and C1 in hold mode.
2	AGND	Analog Ground	26	HOLD $\overline{B}$	Places Channels B0 and B1 in hold mode.
3	DB15	Data Valid Output: "1" for data valid; "0" for invalid data.	27	HOLD $\overline{A}$	Places Channels A0 and A1 in hold mode.
4	DB14	Channel Address Output Pin (see channel truth table)	28	BYTE	2 x 8 Output Capability. Active HIGH
5	DB13	Channel Address Output Pin (see channel truth table)	29	A2	A2 Address/Mode Select Pin (see Address/Mode Truth table).
6	DB12	Channel Address Output Pin (see channel truth table)	30	A1	A1 Address/Mode Select Pin (see Address/Mode Truth Table).
7	DB11	Data Bit 11 - MSB	31	A0	A0 Address/Mode Select Pin (see Address/Mode Truth Table).
8	DB10	Data Bit 10	32	RE $\overline{S}$	Reset Pin
9	DB9	Data Bit 9	33	REFOUT	Reference Out
10	DB8	Data Bit 8	34	REFIN	Reference In
11	DB7	Data Bit 7	35	AGND	Analog Ground
12	DB6	Data Bit 6	36	+V <sub>A</sub>	Analog Power Supply. Normally +5V.
13	DB5	Data Bit 5	37	CH A1+	Noninverting Input Channel A1
14	DB4	Data Bit 4	38	CH A1-	Inverting Input Channel A1
15	DB3	Data Bit 3	39	CH B1+	Noninverting Input Channel B1
16	DB2	Data Bit 2	40	CH B1-	Inverting Input Channel B1
17	DB1	Data Bit 1	41	CH C1+	Noninverting Input Channel C1
18	DB0	Data Bit 0 - LSB	42	CH C1-	Inverting Input Channel C1
19	BUSY	Low when a conversion is in progress.	43	CH C0-	Inverting Input Channel C0
20	DGND	Digital Ground	44	CH C0+	Noninverting Input Channel C0
21	+V <sub>D</sub>	Digital Power Supply, +5VDC	45	CH B0-	Inverting Input Channel B0
22	CLOCK	An external clock must be applied to the CLOCK input.	46	CH B0+	Noninverting Input Channel B0
23	R $\overline{D}$	RD Input. Enables the parallel output when used in conjunction with chip select.	47	CH A0-	Inverting Input Channel A0
24	C $\overline{S}$	Chip Select	48	CH A0+	Noninverting Input Channel A0

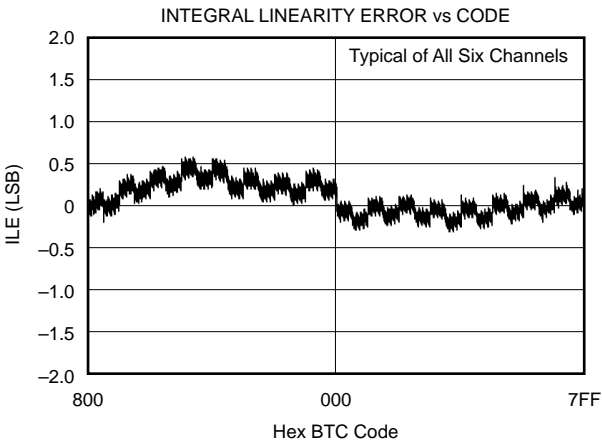
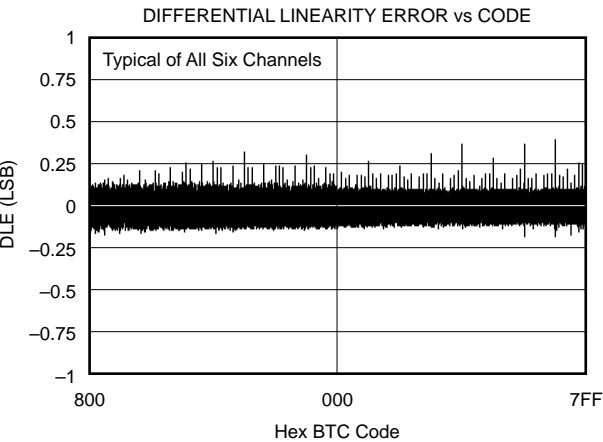
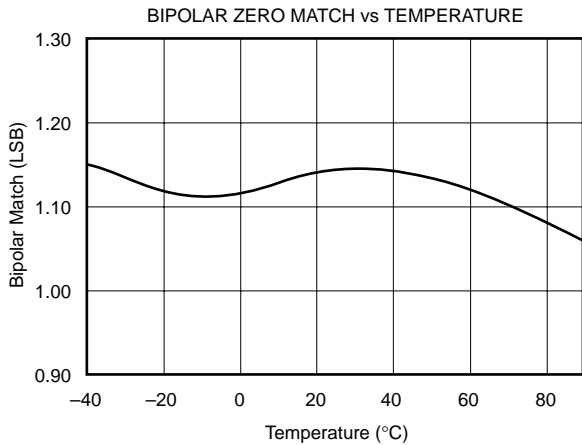
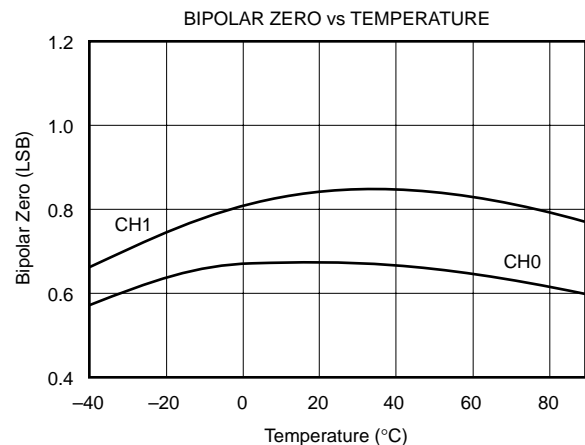
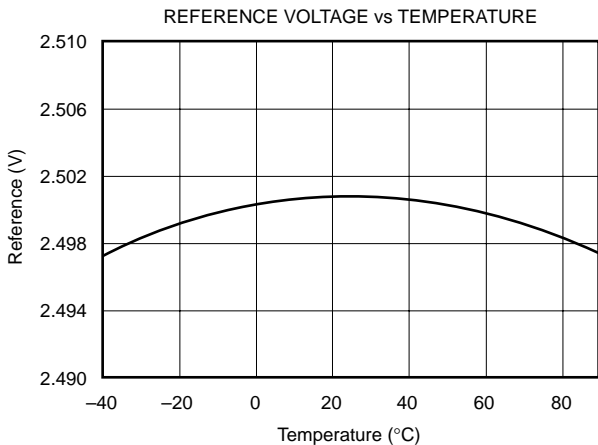
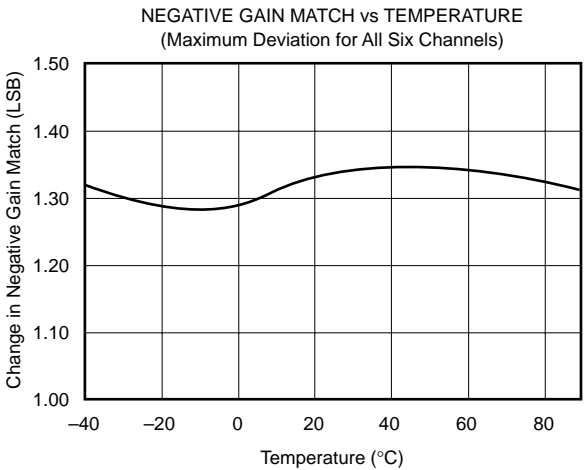
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $+V_A = +V_D = +5\text{V}$ ,  $V_{\text{REF}} = \text{internal } +2.5\text{V}$  and  $f_{\text{CLK}} = 8\text{MHz}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ , unless otherwise noted.



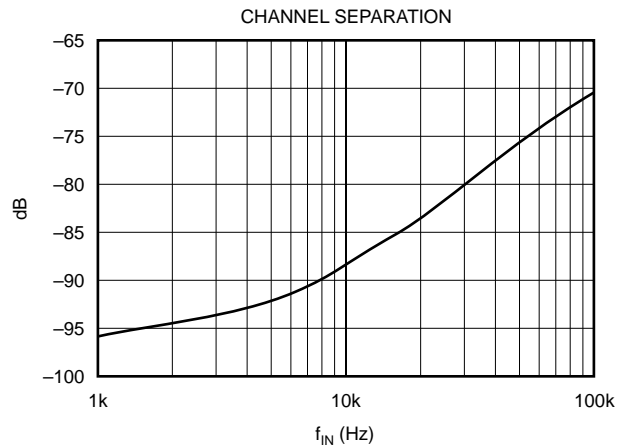
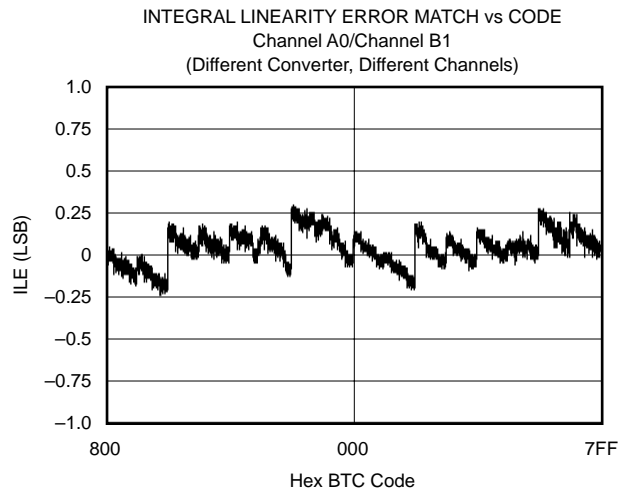
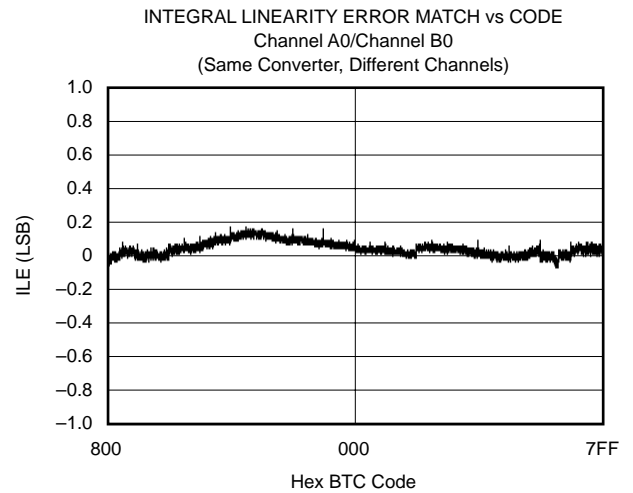
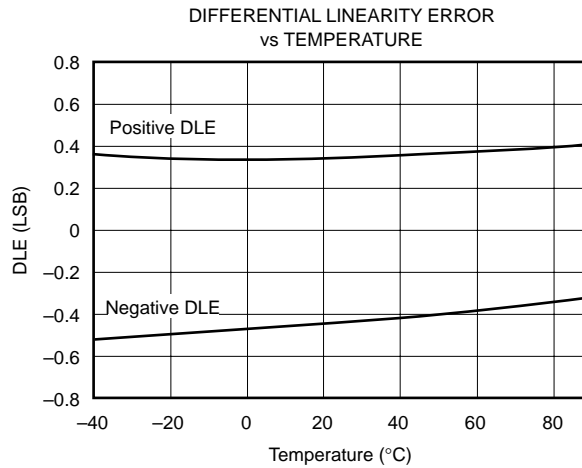
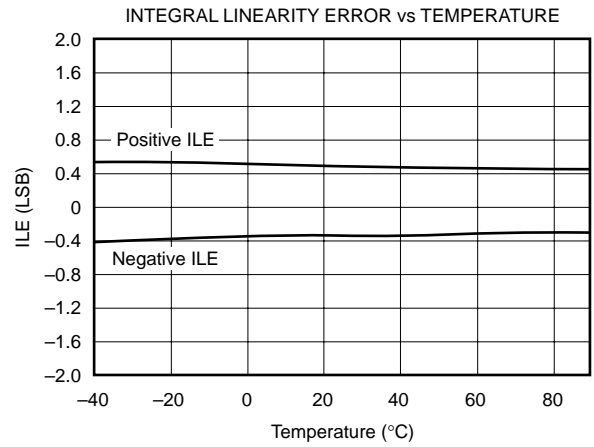
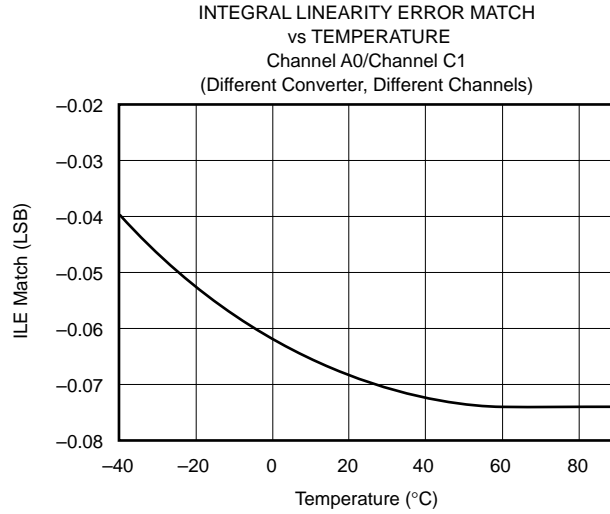
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^{\circ}\text{C}$ ,  $+V_A = +V_D = +5\text{V}$ ,  $V_{\text{REF}} = \text{internal } +2.5\text{V}$  and  $f_{\text{CLK}} = 8\text{MHz}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $+V_A = +V_D = +5\text{V}$ ,  $V_{\text{REF}} = \text{internal } +2.5\text{V}$  and  $f_{\text{CLK}} = 8\text{MHz}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ , unless otherwise noted.



# INTRODUCTION

The ADS7864 is a high speed, low power, dual 12-bit A/D converter that operates from a single +5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The part contains dual 2 $\mu$ s successive approximation ADCs, six differential sample-and-hold amplifiers, an internal +2.5V reference with REF<sub>IN</sub> and REF<sub>OUT</sub> pins and a high speed parallel interface. There are six analog inputs that are grouped into three channels (A, B and C). Each A/D converter has three inputs (A0/A1, B0/B1 and C0/C1) that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. Each pair of channels has a hold signal ( $\overline{\text{HOLDA}}$ ,  $\overline{\text{HOLDB}}$ ,  $\overline{\text{HOLDC}}$ ) to allow simultaneous sampling on all 6 channels. The part accepts an analog input voltage in the range of  $-V_{\text{REF}}$  to  $+V_{\text{REF}}$ , centered around the internal +2.5V reference. The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 7).

A conversion is initiated on the ADS7864 by bringing the  $\overline{\text{HOLDX}}$  pin LOW for a minimum of 15ns.  $\overline{\text{HOLDX}}$  LOW places both sample-and-hold amplifiers of the X channels in the hold state simultaneously and the conversion process is started on both channels. The  $\overline{\text{BUSY}}$  output will then go LOW and remain LOW for the duration of the conversion cycle. The data can be read from the parallel output bus following the conversion by bringing both  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  LOW.

Conversion time for the ADS7864 is 1.75 $\mu$ s when an 8MHz external clock is used. The corresponding acquisition time is 0.25 $\mu$ s. To achieve maximum output rate (500kHz), the read function can be performed during at the start of the next conversion.

NOTE: This mode of operation is described in more detail in the Timing and Control section of this data sheet.

## SAMPLE-AND-HOLD SECTION

The sample-and-hold amplifiers on the ADS7864 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the ADC even when the ADC is operated at its maximum throughput rate of 500kHz. The typical small-signal bandwidth of the sample-and-hold amplifiers is 40MHz.

Typical aperture delay time or the time it takes for the ADS7864 to switch from the sample to the hold mode following the negative edge of  $\overline{\text{HOLDX}}$  signal is 5ns. The average delta of repeated aperture delay values is typically 50ps (also known as aperture jitter). These specifications reflect the ability of the ADS7864 to capture AC input signals accurately at the exact same moment in time.

## REFERENCE

Under normal operation, the REF<sub>OUT</sub> pin (pin 2) should be directly connected to the REF<sub>IN</sub> pin (pin 1) to provide an internal +2.5V reference to the ADS7864. The ADS7864 can operate, however, with an external reference in the range of 1.2V to 2.6V for a corresponding full-scale range of 2.4V to 5.2V.

The internal reference of the ADS7864 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to pin 33 (the internal reference can typically source 2mA of current—load capacitance should not exceed 100pF). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of both CDACs during conversion.

## ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS7864: single-ended or differential (see Figures 1 and 2). When the input is single-ended, the  $-\text{IN}$  input is held at the common-mode voltage. The  $+\text{IN}$  input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode  $+V_{\text{REF}}$ ) and the (common-mode  $-V_{\text{REF}}$ ). The value of  $V_{\text{REF}}$  determines the range over which the common-mode voltage may vary (see Figure 3).

When the input is differential, the amplitude of the input is the difference between the  $+\text{IN}$  and  $-\text{IN}$  input, or:  $(+\text{IN}) - (-\text{IN})$ . The peak-to-peak amplitude of each input is  $\pm 1/2 V_{\text{REF}}$  around this common voltage. However, since the inputs are 180° out of phase, the peak-to-peak amplitude of the differential voltage is  $+V_{\text{REF}}$  to  $-V_{\text{REF}}$ . The value of  $V_{\text{REF}}$  also determines the range of the voltage that may be common to both inputs (see Figure 4).

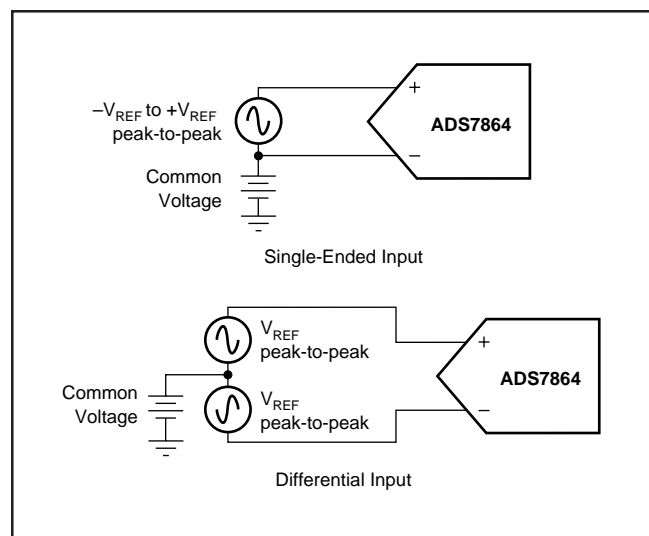


FIGURE 1. Methods of Driving the ADS7864 Single-Ended or Differential.



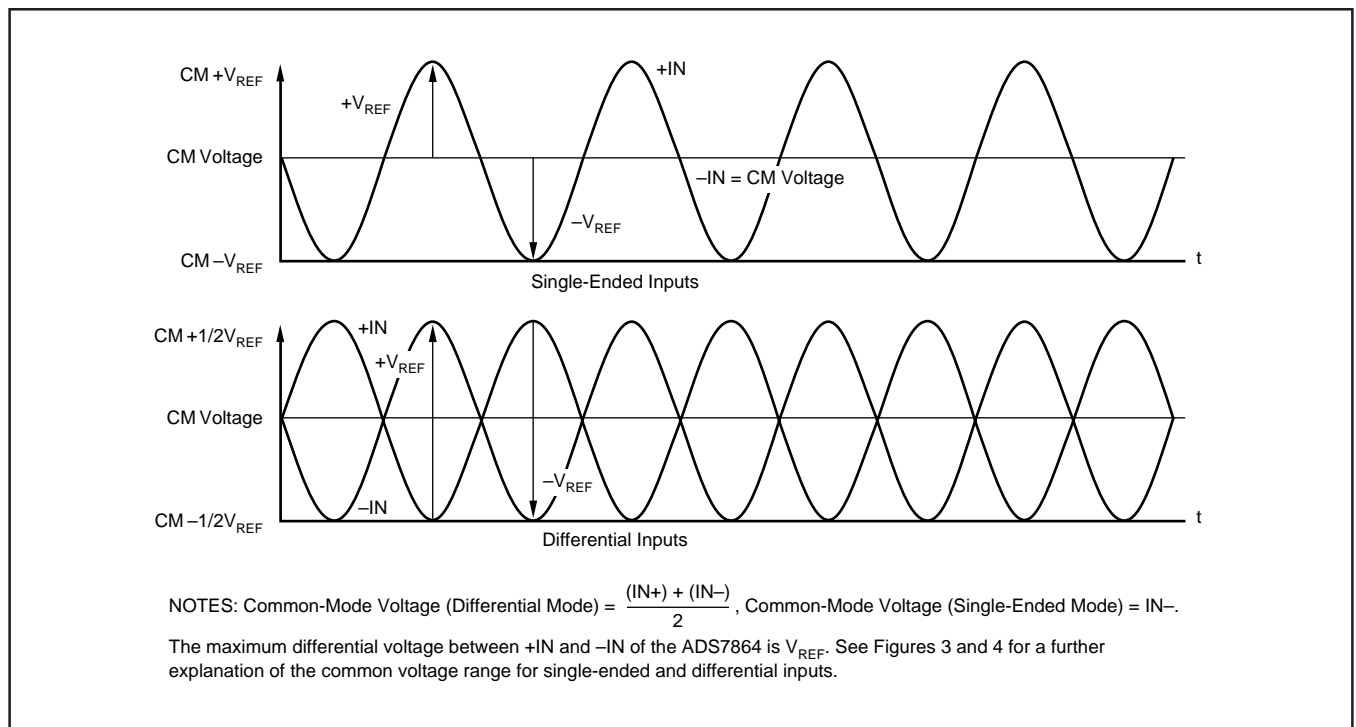


FIGURE 2. Using the ADS7864 in the Single-Ended and Differential Input Modes.

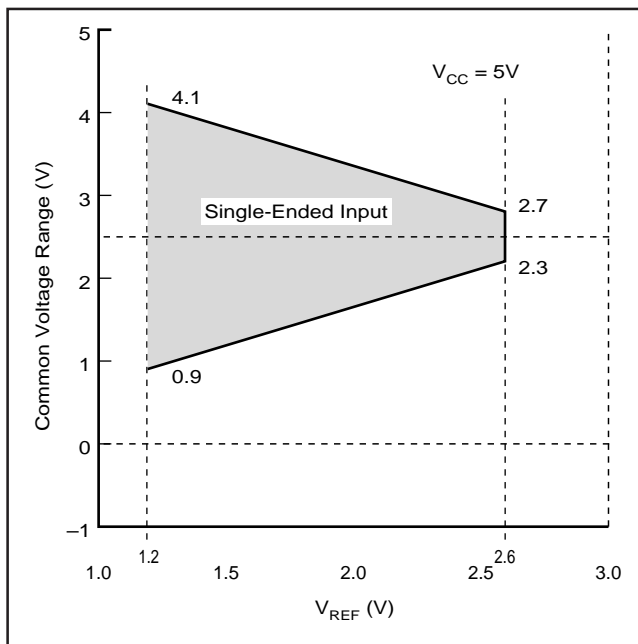


FIGURE 3. Single-Ended Input: Common-Mode Voltage Range vs V<sub>REF</sub>.

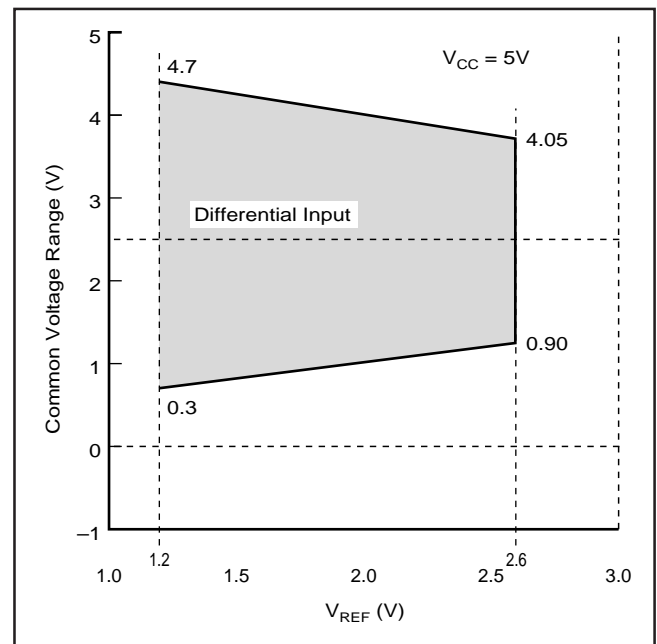


FIGURE 4. Differential Input: Common-Mode Voltage Range vs V<sub>REF</sub>.

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and -IN inputs are matched. Otherwise, this may result in offset error, which will change with both temperature and input voltage.

The input current on the analog inputs depend on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS7864 charges the internal capacitor array during the sampling period. After this

capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (15pF) to a 12-bit settling level within 2 clock cycles. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN and -IN inputs should always remain within the range of GND - 300mV to V<sub>DD</sub> + 300mV.

## TRANSITION NOISE

Figure 5 shows a histogram plot for the ADS7864 following 8,000 conversions of a DC input. The DC input was set at output code 2046. All but one of the conversions had an output code result of 2046 (one of the conversions resulted in an output of 2047). The histogram reveals the excellent noise performance of the ADS7864.

## BIPOLAR INPUTS

The differential inputs of the ADS7864 were designed to accept bipolar inputs ( $-V_{REF}$  and  $+V_{REF}$ ) around the internal reference voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring a single amplifier and four external resistors, the ADS7864 can be configured to except bipolar inputs. The conventional  $\pm 2.5V$ ,  $\pm 5V$ , and  $\pm 10V$  input ranges can be interfaced to the ADS7864 using the resistor values shown in Figure 7.

## TIMING AND CONTROL

The ADS7864 uses an external clock (CLOCK, pin 22) which controls the conversion rate of the CDAC. With an 8MHz external clock, the A/D sampling rate is 500kHz which corresponds to a  $2\mu s$  maximum throughput time.

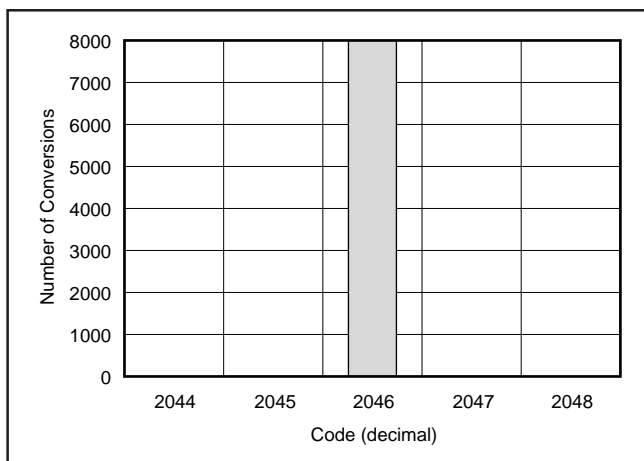


FIGURE 5. Histogram of 8,000 Conversions of a DC Input.

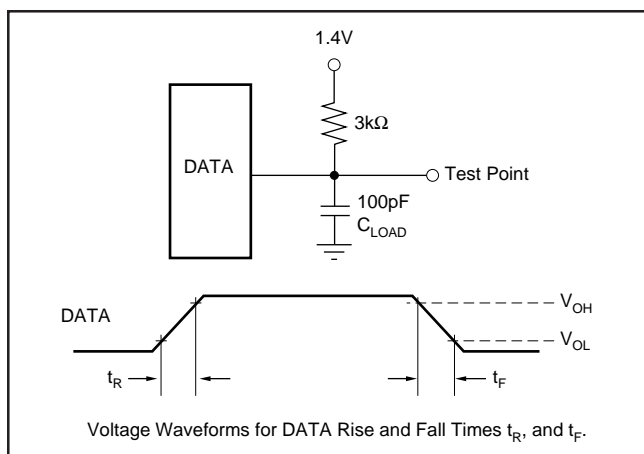


FIGURE 6. Test Circuits for Timing Specifications.

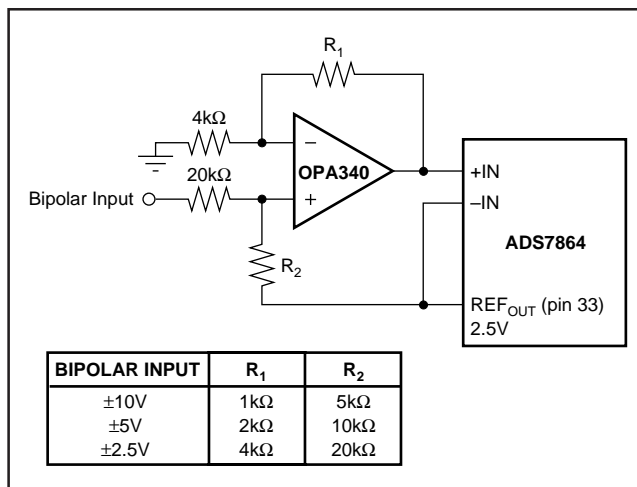


FIGURE 7. Level Shift Circuit for Bipolar Input Ranges.

## THEORY OF OPERATION

The ADS7864 contains two 12-bit A/D converters that operate simultaneously. The three hold signals (HOLDA, HOLDB, HOLDC) select the input MUX and initiate the conversion. A simultaneous hold on all six channels can occur with all three hold signals strobed together. The converted values are saved in 6 registers. For each read operation the ADS7864 outputs 16 bits of information (12 Data, 3 Channel Address and Data Valid). The Address/Mode signals (A0, A1, A2) select how the data is read from the ADS7864. These Address/Mode signals can define a selection of a single channel, a cycle mode that cycles through all channels or a FIFO mode that sequences the data determined by the order of the Hold signals. The FIFO mode will allow the 6 registers to be used by a single channel pair and therefore three locations for CH X0 and three locations for CH X1 can be acquired before they are read from the part.

### EXPLANATION OF CLOCK, RESET AND BUSY PINS

**CLOCK**—An external clock has to be provided for the ADS7864. The maximum clock frequency is 8MHz. The minimum clock cycle is 125ns (Figure 8,  $t_5$ ), and the clock has to remain HIGH (Figure 8,  $t_6$ ) or LOW (Figure 8,  $t_7$ ) for at least 40ns.

**RESET**—Bringing reset LOW will reset the ADS7864. It will clear all the output registers, stop any actual conversions and will close the sampling switches. Reset has to stay LOW for at least 20ns (Figure 8,  $t_8$ ). The reset should be back HIGH for at least 20ns (Figure 8,  $t_9$ ), before starting the next conversion (negative hold edge).

**BUSY**—Busy goes LOW when the internal A/D converters start a new conversion. It stays LOW as long as the conversion is in progress (Figure 9, 13 clock-cycles,  $t_{10}$ ) and rises again, after the data is latched to the output register. With busy going high, the new data can be read. It takes at least 16 clock cycles (Figure 9,  $t_{11}$ ) to complete conversion.

## START OF A CONVERSION

By bringing one or all of the  $\overline{\text{HOLDX}}$  signals low, the input data of the corresponding channel X is immediately placed in the hold mode (5ns). The conversion of this channel X follows as soon as the AD-converter is available for the particular channel. If other channels are already in the hold mode but not converted, then the conversion of channel X is put in the queue until the previous conversion has been completed. If more than one channel goes into hold mode within one clock cycle, then channel A will be converted first if  $\overline{\text{HOLDA}}$  is one of the triggered hold signals. Next channel B will be converted and at last channel C. If it is important to detect a hold command during a certain clock-cycle, then the falling edge of the hold signal has to occur at least 10ns before the falling edge of clock. (Figure 8,  $t_1$ ). The hold signal can remain low without initiating a new conversion. The hold signal has to be high for at least 15ns (Figure 8,  $t_2$ ) before it is brought low again and hold has to stay low for at least 20ns (Figure 8,  $t_3$ ).

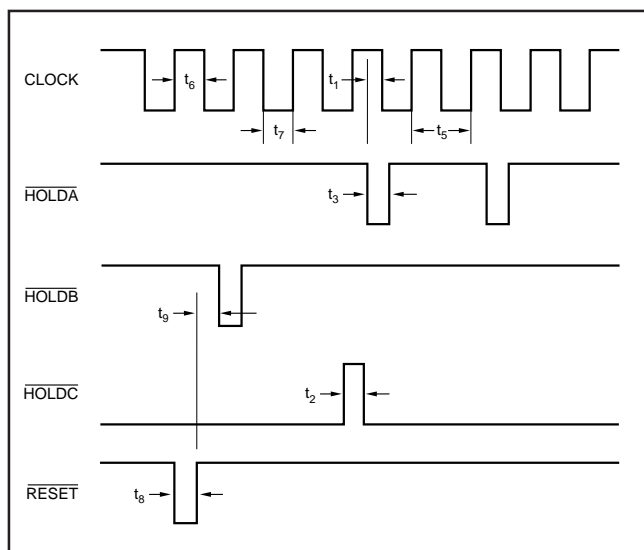


FIGURE 8. Start of the Conversion.

In the example of Figure 8, the signal  $\overline{\text{HOLDB}}$  goes low first and channel B0 and B1 will be converted first. The falling edges of  $\overline{\text{HOLDA}}$  and  $\overline{\text{HOLDC}}$  occur within the same clock cycle. Therefore, the channels A0 and A1 will be converted as soon as the channels B0 and B1 are finished (plus acquisition time). When the A-channels are finished, the C-channels will be converted. The second  $\overline{\text{HOLDA}}$  signal is ignored, as the A-channels are not converted at this point in time.

Once a particular hold signal goes low, further impulses of this hold signal are ignored until the conversion is finished or the part is reset. When the conversion is finished ( $\overline{\text{BUSY}}$  signal goes high) the sampling switches will close and sample the selected channel. The start of the next conversion must be delayed to allow the input capacitor of the ADS7864 to be fully charged. This delay time depends on the driving amplifier, but should be at least 175ns (Figure 9,  $t_4$ ).

The ADS7864 can also convert one channel continuously, as it is shown in Figure 9 with channel B. Therefore,  $\overline{\text{HOLDA}}$  and  $\overline{\text{HOLDC}}$  are kept high all the time. To gain acquisition

## TIMING SPECIFICATIONS

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_1$	HOLD (A, B, C) before falling edge of clock	10			ns
$t_2$	HOLD HIGH time to be recognized again	15			ns
$t_3$	HOLD LOW time	20			ns
$t_4$	Input capacitor charge time	175			ns
$t_5$	Clock period	125			ns
$t_6$	Clock HIGH time	40			ns
$t_7$	Clock LOW time	40			ns
$t_8$	Reset pulse width	20			ns
$t_9$	First hold after reset	20			ns
$t_{10}$	Conversion time		$12.5 \cdot t_5$		ns
$t_{11}$	Successive conversion time ( $16 \cdot t_5$ )	2			$\mu\text{s}$
$t_{12}$	Address setup before $\overline{\text{RD}}$	10			ns
$t_{13}$	$\overline{\text{CS}}$ before end of $\overline{\text{RD}}$	30			ns
$t_{14}$	$\overline{\text{RD}}$ HIGH time	30			ns

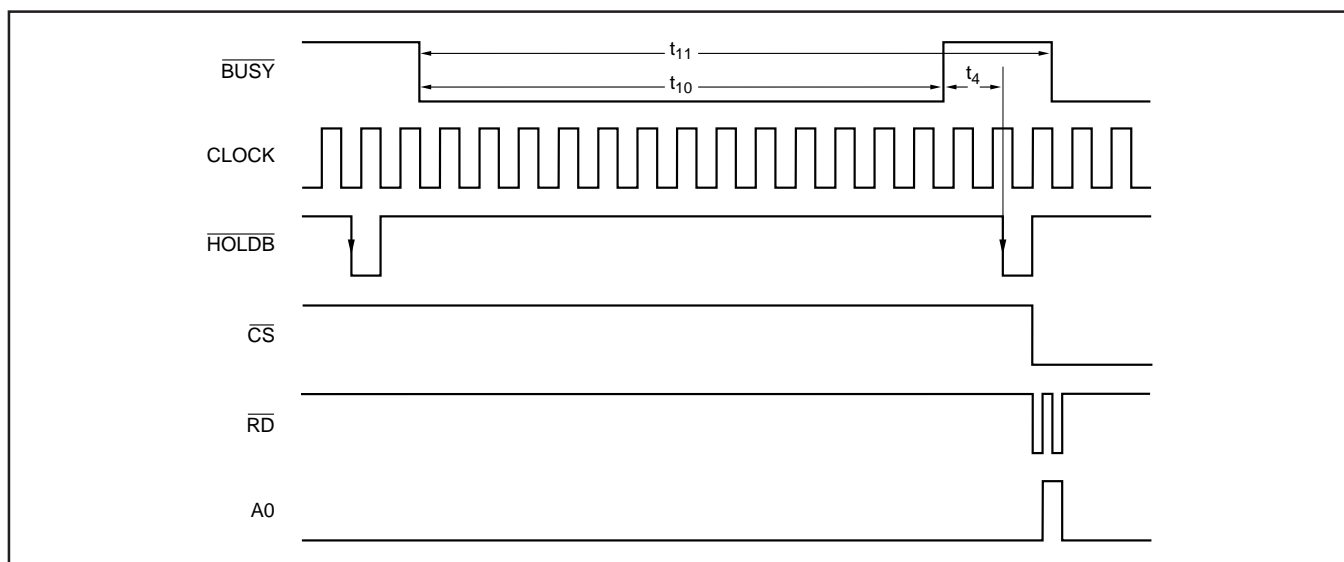


FIGURE 9. Timing of One Conversion Cycle.

time, the falling edge of  $\overline{\text{HOLDB}}$  takes place just before the falling edge of clock. One conversion requires 16 clock cycles. Here, data is read after the next conversion is initiated by  $\overline{\text{HOLDB}}$ . To read data from channel B, A1 is set high and A2 is low. As A0 is low during the first reading (A2 A1 A0 = 010) data B0 is put to the output. Before the second  $\overline{\text{RD}}$ , A0 switches high (A2 A1 A0 = 011) so data from channel B1 is read.

**READING DATA ( $\overline{\text{RD}}$ ,  $\overline{\text{CS}}$ )**—In general, the channel/data outputs are in tristate. Both,  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  have to be LOW to enable these outputs.  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  have to stay LOW together for at least 30ns (Figure 10,  $t_{13}$ ) before the output data is valid.  $\overline{\text{RD}}$  has to remain high for at least 30ns (Figure 10,  $t_{14}$ ) before bringing it back LOW for a subsequent read command.

12.5 clock-cycles after the start of a conversion ( $\overline{\text{BUSY}}$  going LOW), the new data is latched into its output register. If a read process is initiated around 12.5 clock cycles after  $\overline{\text{BUSY}}$  went LOW,  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  should stay LOW for at least 50ns to get the new data stored to its register and switched to the output.

$\overline{\text{CS}}$  being LOW tells the ADS7864 that the bus on the board is assigned to the ADS7864. If an A/D converter shares a bus with digital gates, there is a possibility, that digital (high frequency) noise gets coupled into the A/D converter. If the bus is just used by the ADS7864,  $\overline{\text{CS}}$  can be hardwired to ground. Reading data at the falling edge of one of the hold signals might cause distortion of hold value.

## OUTPUT CODE (DB15...DB0)

The ADS7864 has a 16 bit output word. DB15 is 1 if the output contains valid data. This is important for the FIFO mode. Valid Data can be read until DB15 switches to 0. DB14, DB13 and DB12 store channel information as indicated in Table I (Channel Truth Table). The 12 bit output data is stored from DB11 (MSB) to DB0 (LSB).

DATA CHANNEL	DB14	DB13	DB12
A0	0	0	0
A1	0	0	1
B0	0	1	0
B1	0	1	1
C0	1	0	0
C1	1	0	1

TABLE I. Channel Truth Table.

**BYTE**—If there is only an 8-bit bus available on a board then Byte can be set HIGH (see Figures 11 and 12). In this case, the lower eight bits can be read at the output pins DB7 to DB0 at the first  $\overline{\text{RD}}$  signal and the higher bits after the second  $\overline{\text{RD}}$  signal.

## GETTING DATA

The ADS7864 has three different output modes that are selected with A2, A1 and A0.

With (A2 A1 A0) = 000 to 101 a particular channel can directly be addressed (see Table II and Figure 9). The channel address should be set at least 10ns (Figure 10,  $t_{12}$ ) before the falling edge of  $\overline{\text{RD}}$  and should not change as long as  $\overline{\text{RD}}$  is low.

CHANNEL SELECTED/ MODE	A2	A1	A0
A0	0	0	0
A1	0	0	1
B0	0	1	0
B1	0	1	1
C0	1	0	0
C1	1	0	1
Cycle Mode	1	1	0
FIFO Mode	1	1	1

TABLE II. Address/Mode Truth Table.

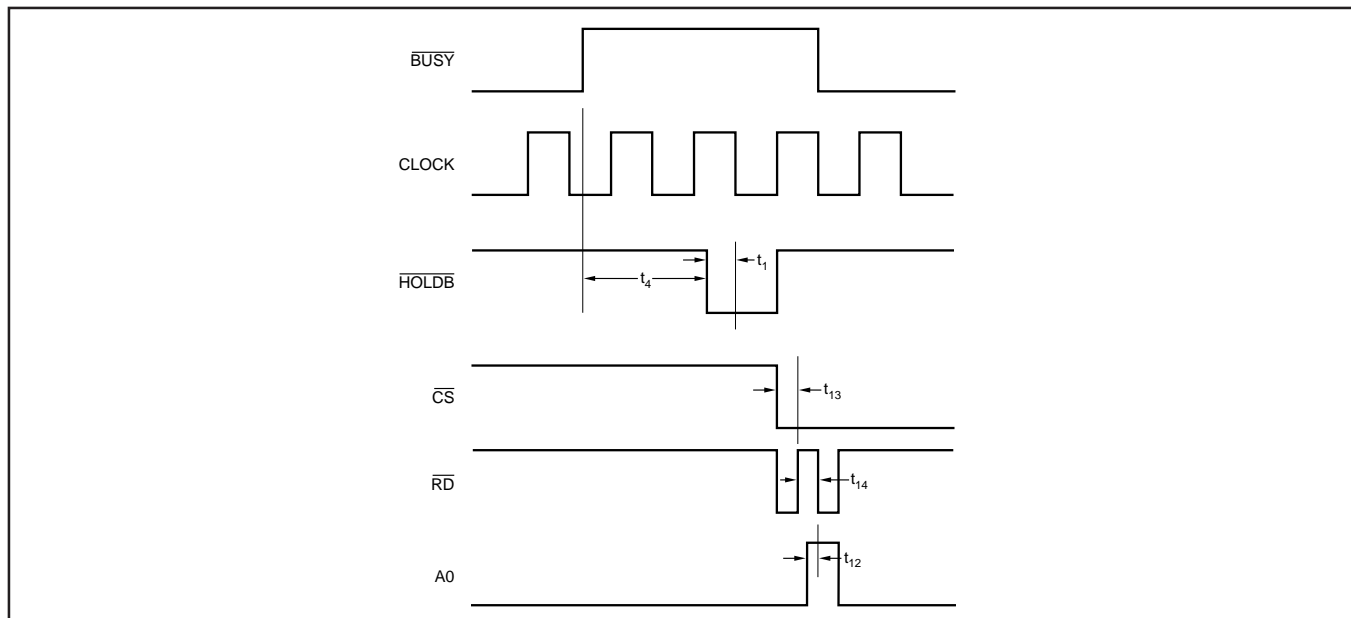


FIGURE 10. Timing for Reading Data.

With (A2 A1 A0) = 110 the interface is running in a cycle mode (see Figures 11 and 12). Here, data from channel A0 is read on the first  $\overline{RD}$  signal, then A1 on the second, followed by B0, B1, C0 and finally C1 before reading A0 again. Data from channel A0 is brought to the output first after a reset-signal or after powering the part up.

The third mode is a FIFO mode that is addressed with (A2 A1 A0 = 111). Data of the channel that is converted first will be read first. So, if a particular channel is most interesting

and is converted more frequently (e.g., to get a history of a particular channel) then there are 3 output registers per channel available to store data.

If a read process is just going on ( $\overline{RD}$  signal low) and new data has to be stored, then the ADS7864 will wait until the read process is finished ( $\overline{RD}$  signal going high) before the new data gets latched into its output register.

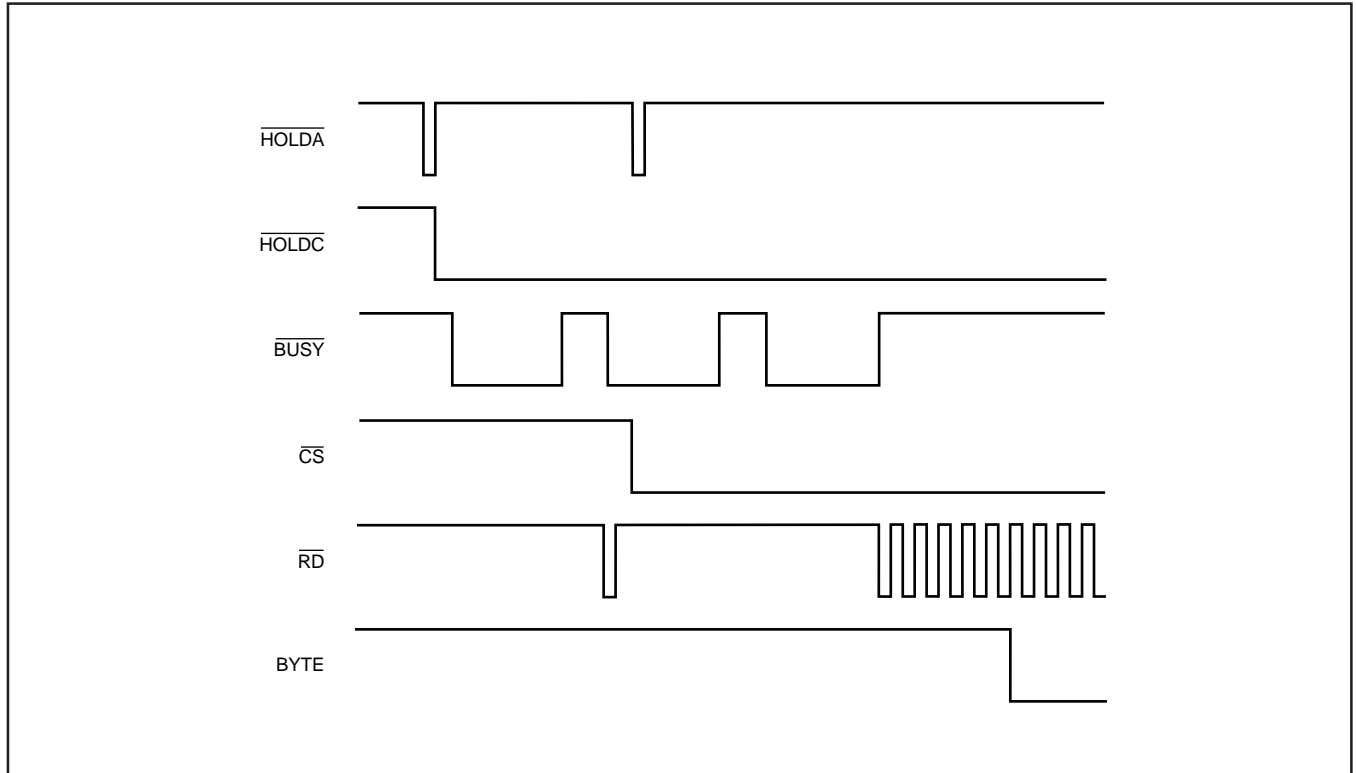


FIGURE 11. Reading Data in Cycling Mode.

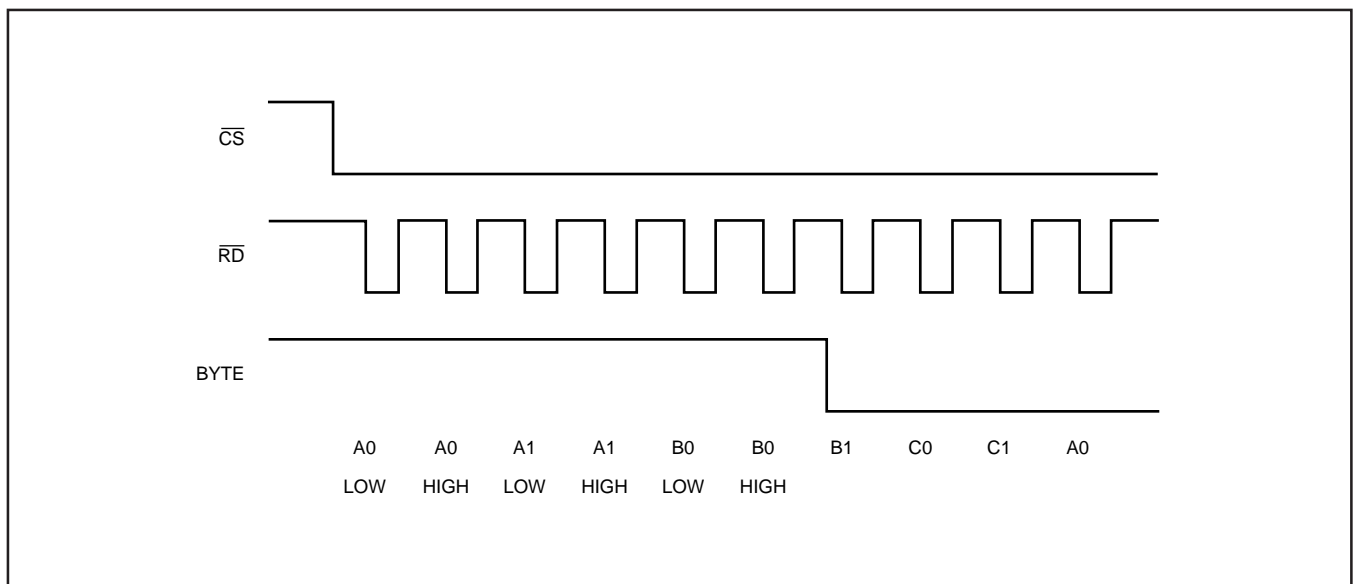


FIGURE 12. Reading Data in Cycling Mode.

At time  $t_A$  (Figure 13) the ADS7864 resets. With the reset signal all conversions and scheduled conversions are cancelled. The data in the output registers are also cleared. With a reset a running conversion gets interrupted and all channels go into the sample mode again.

At time  $t_B$  a  $\overline{\text{HOLDB}}$  signal occurs. With the next falling clock edge ( $t_C$ ) the ADS7864 puts channel B into the loop to be converted next. As the reset signal occurred at  $t_A$ , the conversion of channel B will be started with the next rising edge of the clock after  $t_C$ .

Within the next clock cycle ( $t_C$  to  $t_F$ ),  $\overline{\text{HOLDC}}$  ( $t_D$ ) and  $\overline{\text{HOLDA}}$  ( $t_E$ ) occur. If more than one hold signals get active within one clock cycle, channel A will be converted first. So as soon as the conversion of channel B is done, the conversion of channel A will be initiated. After this second conversion, channel C will be converted.

The 16 bit output word has following structure:

Valid Data	3-Bit Channel Information	12-Bit Data Word
------------	---------------------------	------------------

Bit 15 shows if the FIFO is empty (low) or if it contains channel information (high). Bit 12 to 14 contain the Channel for the 12 bit data word (Bit 0 to 11). If the data is from channel A0, then bits 14 to 12 are 000. The Channel bit pattern is outlined in Table I (Channel Truth Table).

New data is always written into the next available register. At  $t_0$  (see Figure 14), the reset deletes all the existing data. At  $t_1$  the new data of the channels A0 and A1 are put into registers 0 and 1. On  $t_2$  the read process of channel A0 data is finished. Therefore this data is dumped and A1 data is shifted to register 0. At  $t_3$  new data is available, this time from channel B0 and B1. This data is written into the next available registers (register 1 and 2). The new data of channel C0 and C1 at  $t_4$  is put on top (registers 3 and 4).

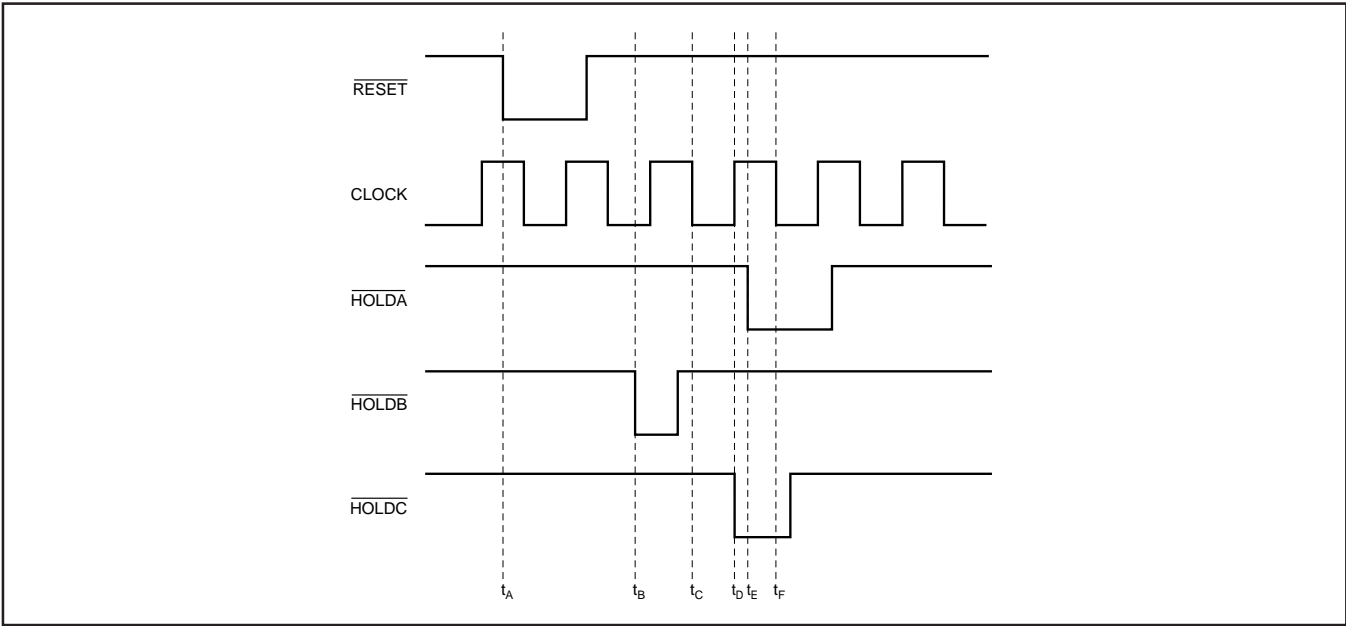


FIGURE 13. Example of Hold Signals.

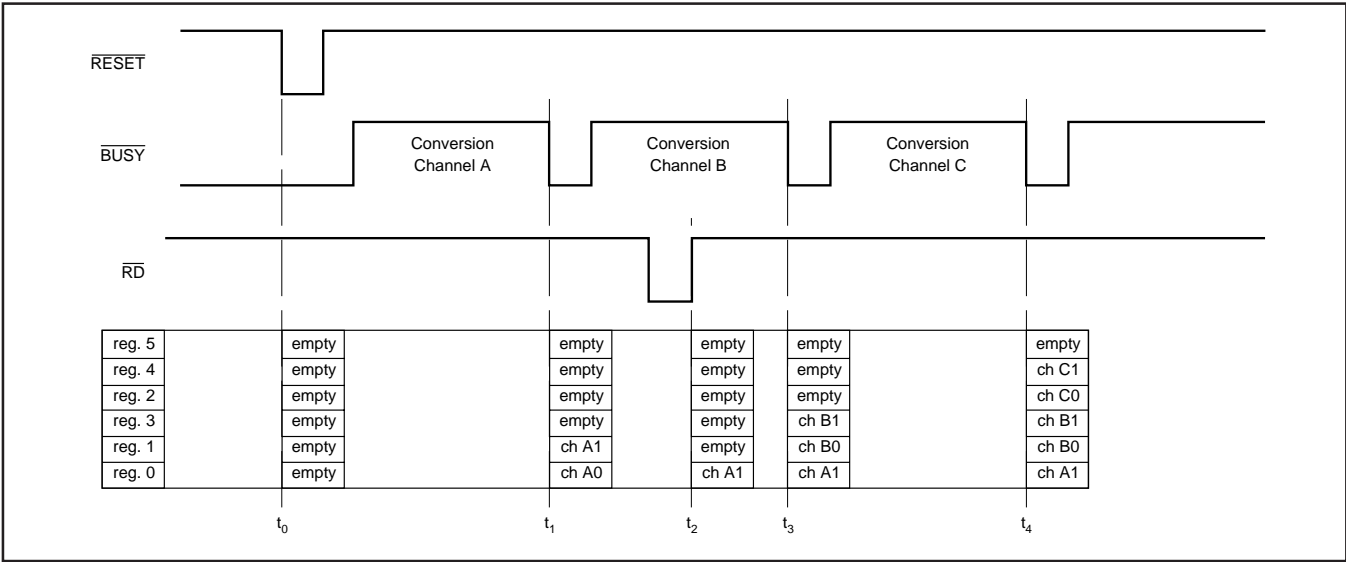


FIGURE 14. Functionality Diagram of FIFO Registers.

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7864 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic or high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. Their error can change if the external event changes in time with respect to the CLOCK input.

With this in mind, power to the ADS7864 should be clean and well bypassed. A 0.1 $\mu$ F ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor is recommended. If needed, an even larger capacitor and a 5 $\Omega$  or 10 $\Omega$  series resistor may be used

to low-pass filter a noisy supply. On average, the ADS7864 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A bypass capacitor must not be used when using the internal reference (tie pin 33 directly to pin 34).

The AGND and DGND pins should be connected to a clean ground point. In all cases, this should be the ‘analog’ ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

## APPLICATIONS

An applications section will be added featuring the ADS7864 interfacing to popular DSP processors. The updated data sheet will be available in the near future on the Burr-Brown web site ([www.burr-brown.com](http://www.burr-brown.com)).

PACKAGE DRAWING

